High-speed CMOS Logic
Data Manual

TEXAS INSTRUMENTS

– European Semiconductor Division –

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HIGH-SPEED CMOS LOGIC DATA MANUAL
1984

Texas Instruments is pleased to announce the SN74HC family of high-speed CMOS logic circuits. This versatile new family promises to be the product family of choice for many new logic systems, offering a unique combination of high-speed, low-power dissipation, high noise immunity, wide fanout capability, extended supply voltage range, and high reliability.

This data book describes the initial product line scheduled for introduction during 1983. Included are pinout and package information, logic symbols, maximum ratings and AC/DC electrical characteristics.

TEXAS INSTRUMENTS HIGH-SPEED CMOS LOGIC
when both, speed and low power are critical

The advanced SN74HC family from Texas Instruments may well become the most widely accepted low-power/high-performance logic family.
It features high speed, low power dissipation, high noise immunity, wide fan-out capability, and high reliability.

With the advent of the SN74HC family. You no longer need to sacrifice speed for reduced power dissipation or vise versa now you can have both in your logic design.

Also important is that the entire SN74HC family is compatible in function and pin out with most other T.I. logic families. This makes board-for-board replacement for existing logic simple and fast.

High speed C-MOS advantages over existing logic TTL Families

- Very low power consumption
- Superior noise immunity
- LS-TTL compatible speed
- TTL input/output level compatibility either direct or via SN74HCT interface devices
- Improved ESD (electrostatic discharge) protection exceeding MIL-STD 883 B
- Available in SN74HC plastic D.I.P. as later on in SN54HC ceramic D.I.P. or the new space saving **P**lastic **L**eaded **C**hip **C**arrier.

GENERAL INFORMATION

ALPHANUMERIC INDEX

* = available 1.Quarter '84
§ = will be announced '84

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TYPE NUMBERS	RATINGS AND CHARACTERISTICS TABLE	RATINGS AND CHARACTERISTICS PAGE	DESCRIPTIVE INFORMATION PAGE	TYPE NUMBERS	RATINGS AND CHARACTERISTICS TABLE	RATINGS AND CHARACTERISTICS PAGE	DESCRIPTIVE INFORMATION PAGE
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§ = will be announced '84

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (See individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

* Current out of a terminal is given as a negative value.

GLOSSARY
SYMBOLS, TERMS, AND DEFINITIONS

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. ($t_{dis} = t_{PHZ}$ or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). ($t_{en} = t_{PZH}$ or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time**
Transition time, low-to-high-level, $t_{TLH} = t_r$
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, $t_{THL} = t_f$
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

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GATES WITH OPEN-DRAIN OUTPUTS

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AND, NAND GATES AND INVERTERS

(for Maximum Ratings and Electrical Characteristics See Table I, Page 3-3)

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(for Maximum Ratings and Electrical Characteristics See Table I, Page 3-3)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
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OR, NOR, EXCLUSIVE-OR, AND AND-OR-INVERT GATES

(for Maximum Ratings and Electrical Characteristics See Table I, Page 3-3)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
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(for Maximum Ratings and Electrical Characteristics See Table III, Page 3-6)

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Hex Bus Drivers/Receivers	True	Common Enables	'HC365	4-106
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Octal Bus Drivers/Receivers	Inverting	Symmetrical Enables	'HC240	4-83
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Octal Bus Transceivers	Inverting	Independent Enables for A and B Buses	'HC620	4-133
	True		'HC623	
	Inverting	Enable and Direction Control	'HC640	4-137
	True and Inverting		'HC643	
	True		'HC645	
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Octal Bus Transceivers with Registers	True	Enable and Direction Control	'HC646	
	Inverting		'HC648	
	Inverting	Independent Enables for A and B Buses	'HC651	
	True		'HC652	

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D-TYPE FLIP-FLOPS

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Hex D-Type Flip-flops with Common Clocks	Q only	Common Clear	'HC174	IV	3-8	4-71
		Output Enable	'HC378			4-114
Octal D-type Flip-flops with Common Clocks	Q only	Common Clear	'HC273			4-98
		Output Enable	'HC377			4-114
	3-State, Q only	Output Control	'HC374	III	3-6	4-111
			'HC574			
	3-State, $\overline{Q}$ only	Output Control	'HC534			
			'HC564			

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(for Maximum Ratings and Electrical Characteristics See Table II, Page 3-5)

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	Q only	'HC77			
Quad D-type Registers	Q only, 3-state	'HC173	III	3-6	
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		'HC573			4-130
	$\overline{Q}$ only, 3-state	'HC533			4-124
		'HC563			4-127
8-Bit Addressable Latches	Q only	'HC4724	IV	3-8	
		'HC259			

MONOSTABLE MULTIVIBRATORS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 3-8)

DESCRIPTION	FEATURES		DEVICE TYPE	DESCRIPTIVE INFORMATION
Dual Monostable Multivibrators with Direct Clear, Postive and Negative Inputs, and complementary Outputs			'HC221	
	Retriggerable		'HC123	
		Will not trigger from clear	'HC423	
			'HC4538	

SHIFT REGISTERS

DESCRIPTION	INPUTS	OUTPUTS	DEVICE TYPE	RATINGS AND CHARACTERISTIC TABLE	RATINGS AND CHARACTERISTIC PAGE	DESCRIPTIVE INFORMATION
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4-Bit Bidirectional Shift Registers with Clear	Serial/Parallel	Parallel	'HC194			
8-Bit Shift Registers	Serial/Parallel, Clock Inhibit, Shift/Load	2 Serial	'HC165			4-65
	2 Serial, Clear	Parallel	'HC164			4-62
	Serial/Parallel, Clear, Clock Inhibit, Shift/Load	Serial	'HC166			4-68
8-Bit Shift Registers with Input Registers	Serial/Parallel	Serial	'HC597			
	Serial/Parallel	3-state Parallel (Multiplexed I/O)	'HC598			
8-Bit Bidirectional Shift Registers with Storage and Multiplexed 3-State I/O	Serial/Parallel	3-state Parallel	'HC299	III	3-6	
			'HC323			
8-Bit Shift Registers with Output Registers	Serial	Parallel	'HC594			
		3-State Parallel	'HC595			

SYNCHRONOUS COUNTERS

DESCRIPTION	FEATURES		TYPE	RATINGS AND CHARACTERISTICS TABLE	RATINGS AND CHARACTERISTICS PAGE	DESCRIPTIVE INFORMATION
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Divide-by-10 Johnson Counter	Async Clear		'HC4017			
4-Bit Binary	Async Clear	Sync Load	'HC161			4-55
	Sync Clear		'HC163			4-55
4-Bit Binary Up/Down	Clock Inhibit	Async Load	'HC191			4-74
	Async Clear		'HC193			4-79
8-Bit Binary with Input Registers	Sync Clear		'HC592			
		Multiplexed 3-state I/O	'HC593	III	3-6	
8-Bit Binary with Output Registers	Sync Clear	3-state Outputs	'HC590			

ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 3-8)

DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
12-Bit Binary Counters		'HC4040	
14-Bit Binary Counters		'HC4020	
	On-chip Oscillator	'HC4060	
Dual Decade Counters	Bi-quinary or BCD	'HC390	4-119
	Set-to-9 Input	'HC490	4-122
Dual 4-Bit Binary Counters		'HC393	4-119

COMPARATORS, PARITY GENERATORS/ CHECKERS, AND PRIORITY ENCODERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 3-8)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
4-Bit Magnitude Comparators	'HC85	
8-Bit Magnitude Comparators	'HC688	
9-Bit Odd/Even Parity Generator/Checker	'HC280	4-100
10-Line Decimal to 4-Line BCD Priority Encoder	'HC147	

DATA SELECTORS/MULTIPLEXERS

(for Maximum Ratings and Electrical Characteristics See Table III, Page 3-6)

DESCRIPTION	INPUTS	OUTPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
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	Transparent Latches, Enable	Complementary 3-state	'HC354	
	Registers, Enable		'HC356	
Dual 4-line-to-1-Line	Independent Enables	True, 3-state	'HC253	4-93
		Inverting, 3-state	'HC353	4-104
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Quad 2-Line-to-1-Line	Common Enable	True	'HC157	4-52
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		True, 3-state	'HC257	4-95
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DECODERS/DEMULTIPLEXERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 3-8)

DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
4-Line-to-16-Line	2 Enables	'HC154	
	Input latches, Output Enable	'HC4514	
		'HC4515	
4-Line-to-10-Line, BCD-to-Decimal		'HC42	4-18
3-Line-to-8-Line	3 Enables	'HC138	4-42
	3 Enables, Address Latches	'HC137	4-40
Dual 2-Line-to-4-Line	Independent Enables	'HC139	4-44

DISPLAY DECODERS/DRIVERS

DESCRIPTION	DEVICE TYPE	RATINGS AND CHARACTERISTICS		DESCRIPTIVE INFORMATION
		TABLE	PAGE	
BCD-to-7-Segment Decoders/Drivers with Input Latches	'HC4511	IV	3-8	

RANDOM ACCESS MEMORIES

DESCRIPTION	ORGANIZATION	FEATURES	DEVICE TYPE	RATINGS AND CHARACTERISTICS		DESCRIPTIVE INFORMATION
				TABLE	PAGE	
64-Bit	16 x 4	3-state Outputs	'HC189	III	3-6	

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↑ or ↓
⎍	=	one high-level pulse
⎴	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains, H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74HC194.

FUNCTION TABLE

INPUTS											OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL					Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D					
L	X	X	X	X	X	X	X	X	X		L	L	L	L
H	X	X	L	X	X	X	X	X	X		Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d		a	b	c	d
H	L	H	↑	X	H	X	X	X	X		H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X		L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X		Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X		Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X		Q_{An}	Q_{Bn}	Q_{Cn}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

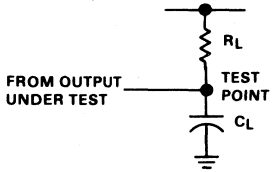
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

Parameter Measurement Information

PARAMETER MEASUREMENT INFORMATION

TOTEM POLE OUTPUTS



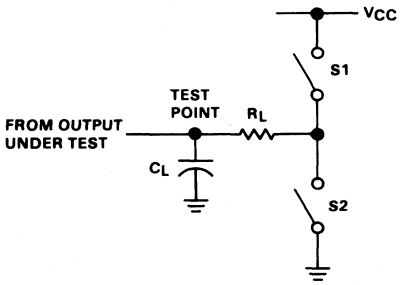
PARAMETER		R_L	C_L†
t_{PLH} or t_{PHL}	Standard outputs	∞	50 pF
	High-current outputs§	∞	50 pF or 150 pF

† C_L includes probe and test fixture capacitance.
§ High-current outputs are indicated by ▷ in the logic symbol.

OPEN-DRAIN OUTPUTS:

The load values for open-drain outputs are as follows:
$R_L = 1k\Omega$ to V_{CC}
$C_L = 50$ pF to GND

3-STATE OUTPUTS



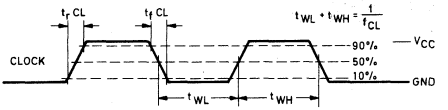
LOAD CIRCUIT

PARAMETER	R_L	C_L†	S_1	S_2
t_{PZH}	1 k	50 pF or 150 pF	OPEN	CLOSED
t_{PZL}			CLOSED	OPEN
t_{PHZ}	1 k	50 pF	OPEN	CLOSED
t_{PLZ}			CLOSED	OPEN
t_{PLH} or t_{PLH}		50 pF or 150 pF	OPEN	CLOSED

† C_L includes probe and test fixture capacitance.

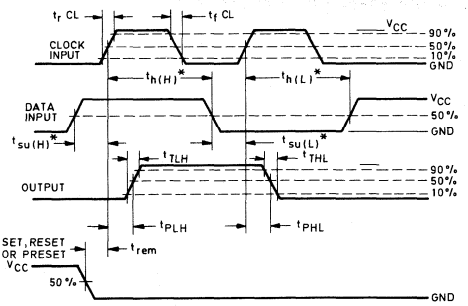
1.0 SWITCHING WAVEFORMS FOR THE 54/74HCXXX AND 54/74HCUXXX

CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{max}, INPUT DUTY CYCLE = 50%

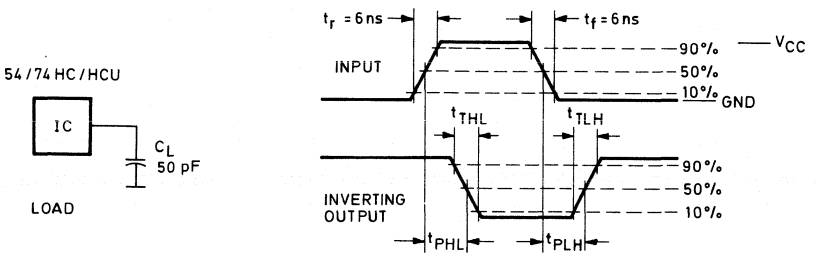
SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE-TRIGGERED SEQUENTIAL LOGIC CIRCUITS.



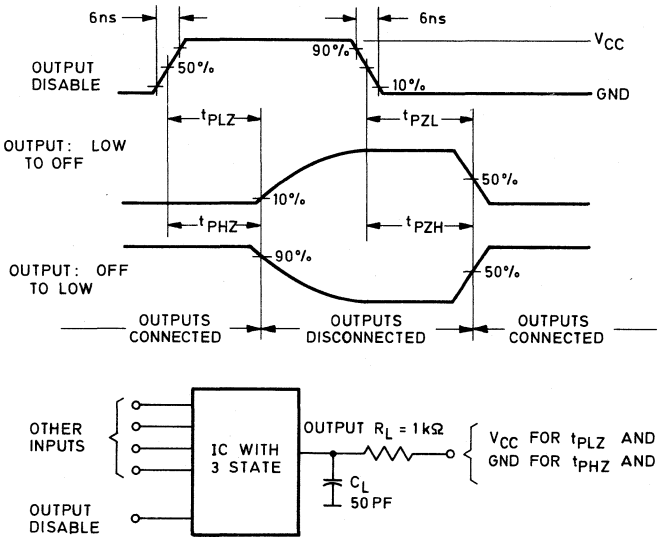
All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

*(H) OR (L) OPTIONAL

TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



54/74HCXXXX THREE-STATE WAVEFORMS AND TEST CIRCUIT



OPEN-DRAIN WAVEFORMS:

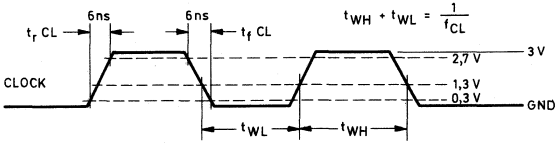
Output R_L = 1kΩ to V_{CC}; C_L = 50 pF

t_{PLZ}, t_{PZL}, wave forms are the same as 3-state

All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

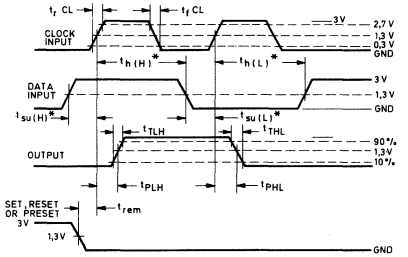
2.0 SWITCHING WAVEFORMS FOR 54/74HCTXXX

CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



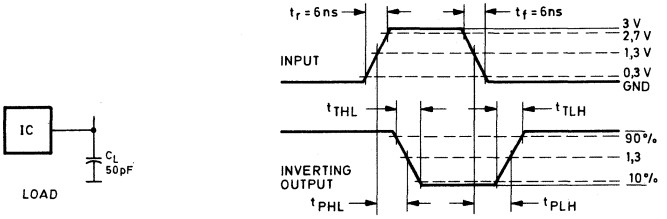
Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{max}, INPUT DUTY CYCLE = 50%

SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE-TRIGGERED SEQUENTIAL LOGIC CIRCUITS

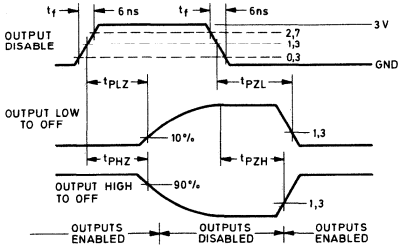


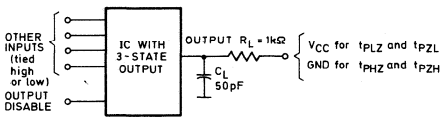
*(H) OR (L) OPTIONAL

TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



54/74HCTXXXX THREE-STATE WAVEFORMS AND TEST CIRCUIT





OPEN-DRAIN WAVEFORMS:

Output R_L = 1kΩ to V_{CC}; C_L = 50 pF

t_{PLZ}, t_{PZL} wave forms are the same as 3-state

Maximum Ratings, Recommended Operating Conditions, and electrical Characteristics

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance citcuits.

Unused inputs must always be connected to an appropriate logic voltage level preferably either V_{CC} or ground.

TABLE I
SPECIFICATIONS FOR SSI CIRCUITS

D2684, DEZEMBER 1982

absolute maximum ratings over operating free-air temperature range†

	MIN	MAX	UNIT
V_{CC}, Supply voltage range	−0.5	7.0	V
V_I, Input voltage range	−0.5	V_{CC}+0.5	V
I_{IK}, Input diode current, peak	−20	20	mA
V_O, Output voltage range	−0.5	V_{CC}+0.5	V
I_{OK}, Output diode current, peak	−20	20	mA
I_O, Output current	−25	25	mA
V_{CC}, Or GND current	−50	50	mA
Lead temperature: J package		300	°C
N package		260	°C
Storage temperature	−65	150	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	PARAMETER	V_{CC}	54HC			74HC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2.0	5.0	6.0	2.0	5.0	6.0	V
V_{IH}	High-level input voltage	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	2.0 4.5 6.0	0 0 0		0.3 0.9 1.2	0 0 0		0.3 0.9 1.2	V
V_I/V_O	Input/Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	4.5 6.0		−4 −5.2			−4 −5.2		mA
I_{OL}	Low-level output current	4.5 6.0		4 5.2			4 5.2		mA
t_t	Input transition (rise and fall) times (except Schmitt-trigger inputs)	2.0 4.5 6.0	0 0 0		1000 500 400	0 0 0		1000 500 400	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	T_A=25°C			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_{IH} or V_{IL}	I_O = −20 μA	2.0 4.5 6.0	1.9 4.4 5.9			1.9 4.4 5.9		1.9 4.4 5.9		V
		I_O = −4 mA I_O = −5.2 mA	4.5 6.0	3.86 5.36			3.7 5.2		3.76 5.26		
V_{OL}	V_{IH} or V_{IL}	I_O = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_O = 4 mA I_O = 5.2 mA	4.5 6.0			0.32 0.32		0.4 0.4		0.37 0.37	
I_I	V_I = V_{CC} or GND		6.0			±0.1		±1.0		±1.0	μA
V_{T+}			2.0 4.5 6.0	0.8 2.0 2.5	1.2 2.5 3.3	1.5 3.15 4.2					V
V_{T-}			2.0 4.5 6.0	0.3 0.9 1.2	0.6 1.6 2.0	0.8 2.0 2.5					V

TABLE I
SPECIFICATIONS FOR SSI CIRCUITS

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	$T_A = 25°C$			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}			2.0	0.2	0.5	1.0					V
–			4.5	0.4	0.7	1.4					
V_{T-}			6.0	0.5	0.8	1.7					
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$		6.0			2.0		40.0		20.0	μA
C_I					3.0	10.0		10.0		10.0	pF

switching characteristics

See individual circuit pages

3

TABLE II
SPECIFICATIONS FOR DUAL AND QUAD FLIP-FLOP AND LATCHES

D2684, DEZEMBER 1982

absolute maximum ratings over operating free-air temperature range†

	MIN	MAX	UNIT
V_{CC}, Supply voltage range	−0.5	7.0	V
V_I, Input voltage range	−0.5	V_{CC}+0.5	V
I_{IK}, Input diode current, peak	−20	20	mA
V_O, Output voltage range	−0.5	V_{CC}+0.5	V
I_{OK}, Output diode current, peak	−20	20	mA
I_O, Output current	−25	25	mA
V_{CC}, Or GND current	−50	50	mA
Lead temperature: J package		300	°C
N package		260	°C
Storage temperature	−65	150	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	PARAMETER	V_{CC}	54HC			74HC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2.0	5.0	6.0	2.0	5.0	6.0	V
V_{IH}	High-level input voltage	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	2.0 4.5 6.0	0 0 0		0.3 0.9 1.2	0 0 0		0.3 0.9 1.2	V
V_I/V_O	Input/Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	4.5 6.0		−4 −5.2			−4 −5.2		mA
I_{OL}	Low-level output current	4.5 6.0		4 5.2			4 5.2		mA
t_t	Input transition (rise and fall) times (except Schmitt-trigger inputs)	2.0 4.5 6.0	0 0 0		1000 500 400	0 0 0		1000 500 400	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	Conditions	V_{CC}	T_A=25C°			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_{IH} or V_{IL}	I = −20 μA	2.0 4.5 6.0	1.9 4.4 5.9			1.9 4.4 5.9		1.9 4.4 5.9		V
		I = −4 mA I = −5.2 mA	4.5 6.0	3.86 5.36			3.7 5.2		3.76 5.26		
V_{OL}	V_{IH} or V_{IL}	I_O = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_O = 4 mA I_O = 5.2 mA	4.5 6.0			0.32 0.32		0.4 0.4		0.37 0.37	
I_I	V_I = V_{CC} or GND		6.0			±0.1		±1.0		±1.0	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0		6.0			4.0		80.0		40.0	μA
C_I					3.0	10.0		10.0		10.0	pF

switching characteristics

See individual circuit pages.

TABLE III
SPECIFICATIONS FOR CIRCUITS WITH HIGH-CURRENT OUTPUTS

D2684, DEZEMBER 1982

absolute maximum ratings over operating free-air temperature range†

	MIN	MAX	UNIT
V_{CC}, Supply voltage range	−0.5	7.0	V
V_I, Input voltage range	−0.5	V_{CC}+0.5	V
I_{IK}, Input diode current, peak	−20	20	mA
V_O, Output voltage range	−0.5	V_{CC}+0.5	V
I_{OK}, Output diode current, peak	−20	20	mA
I_O, Output current	−35	35	mA
V_{CC}, Or GND current	−70	70	mA
Lead temperature: J package		300	°C
N package		260	°C
Storage temperature	−65	150	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	PARAMETER	V_{CC}	54HC			74HC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2.0	5.0	6.0	2.0	5.0	6.0	V
V_{IH}	High-level input voltage	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	2.0 4.5 6.0	0 0 0		0.3 0.9 1.2	0 0 0		0.3 0.9 1.2	V
V_I/V_O	Input/Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-current outputs $	4.5 6.0		−6 −7.8			−6 −7.8	−6	mA
	Standard outputs	4.5 6.0		−4 −5.2			−4 −5.2		
I_{OL}	High-current outputs $	4.5 6.0		6 5.2			6 7.8		mA
	Standard outputs	4.5 6.0		4 5.2			4 5.2		
t_t	Input transition (rise and fall) times	2.0 4.5 6.0	0 0 0		1000 500 400	0 0 0		1000 500 400	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

$ High-current outputs are indicated by the ▷ in the logic symbol. All 3-State outputs are high-current outputs.

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	T_A=25°C			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_{IH} or V_{IL}	I_O = −20 μA	2.0 4.5 6.0	1.9 4.4 5.9			1.9 4.4 5.9		1.9 4.4 5.9		V
		I_O = Note 1 I_O = Note 2	4.5 6.0	3.86 5.36			3.7 5.2		3.76 5.26		
V_{OL}	V_{IH} or V_{IL}	I_O = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_O = Note 3 I_O = Note 4	4.5 6.0			0.32 0.32		0.4 0.4		0.37 0.37	

TABLE III
SPECIFICATIONS FOR CIRCUITS WITH HIGH-CURRENT OUTPUTS

D2684, DECEMBER 1982

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	$T_A = 25C°$			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	$V_I = V_{CC}$ or GND		6.0			±0.1		±1.0		±1.0	μA
I_{OZ}	$V_O = V_{CC}$ or GND $V_I = V_{IH}$ or V_{IL}		6.0			±0.5		±10.0		±5.0	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = O$		6.0			8.0		160.0		80.0	μA
C_I	Except TXCVR I/0				3.0	10.0		10.0		10.0	pF

Notes:
1. $I_O = -4.0$ mA for standard outputs.
   $I_O = -6.0$ mA for high-current outputs.
2. $I_O = -5.2$ mA for standard outputs.
   $I_O = -7.8$ mA for high-current outputs.
3. $I_O = 4.0$ mA for standard outputs.
   $I_O = 6.0$ mA for high-current outputs.
4. $I_O = 5.2$ mA for standard outputs.
   $I_O = 7.8$ mA for high-current outputs.

switching characteristics

See individual circuit pages.

3

absolute maximum ratings over operating free-air temperature range†

	MIN	MAX	UNIT
V_{CC}, Supply voltage range	−0.5	7.0	V
V_I, Input voltage range	−0.5	V_{CC}+0.5	V
I_{IK}, Input diode current, peak	−20	20	mA
V_O, Output voltage range	−0.5	V_{CC}+0.5	V
I_{OK}, Output diode current, peak	−20	20	mA
I_O, Output current	−25	25	mA
V_{CC}, Or GND current	−50	50	mA
Lead temperature: J package		300	°C
N package		260	°C
Storage temperature	−65	150	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	PARAMETER	V_{CC}	54HC			74HC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2.0	5.0	6.0	2.0	5.0	6.0	V
V_{IH}	High-level input voltage	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	2.0 4.5 6.0	0 0 0		0.3 0.9 1.2	0 0 0		0.3 0.9 1.2	V
V_I/V_O	Input/Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	4.5 6.0		−4 −5.2			−4 −5.2		mA
I_{OL}	Low-level output current	4.5 6.0		4 5.2			4 5.2		mA
t_t	Input transition (rise and fall) times (except Schmitt-trigger inputs)	2.0 4.5 6.0	0 0 0		1000 500 400	0 0 0		1000 500 400	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	T_A=25C°			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_{IH} or V_{IL}	I_O = −20 μA	2.0 4.5 6.0	1.9 4.4 5.9			1.9 4.4 5.9		1.9 4.4 5.9		V
		I_O = −4 mA I_O = −5.2 mA	4.5 6.0	3.86 5.36			3.7 5.2		3.76 5.26		
V_{OL}	V_{IH} or V_{IL}	I_O = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_O = 4 mA I_O = 5.2 mA	4.5 6.0			0.32 0.32		0.4 0.4		0.37 0.37	
I_I	V_I = V_{CC} or GND		6.0			±0.1		±1.0		±1.0	μA
I_S (off)	(Analog Switches only) V_I = V_{CC} or GND V_S = ±V_{CC}		6.0			±0.1		±1.0		±1.0	μA
V_{T+}			2.0 4.5 6.0	0.8 2.0 2.5	1.2 2.5 3.3	1.5 3.15 4.2					V

TABLE IV
SPECIFICATIONS FOR MSI CIRCUITS

electrical characteristics over recommended temperature and voltage range (unless otherwise noted)

PARAMETER	V_I	CONDITIONS	V_{CC}	T_A=25C°			54HC		74HC		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T-}			2.0 4.5 6.0	0.3 0.9 1.2	0.6 1.6 2.0	0.8 2.0 2.5					V
V_{T+} − V_{T-}			2.0 4.5 6.0	0.2 0.4 0.5	0.5 0.7 0.8	1.0 1.4 1.7					V
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$		6.0			8.0		160.0		80.0	μA
C_I					3.0	10.0		10.0		10.0	pF

switching characteristics

See individual circuit pages.

3

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Descriptive Information

4

TYPES SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

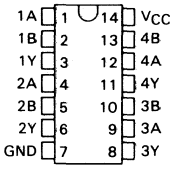
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC00 is characterized for operation from −40°C to 85°C.

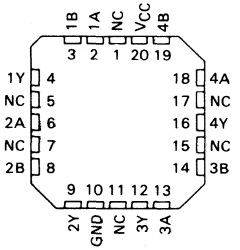
SN54HC00 . . . J PACKAGE
SN74HC00 . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

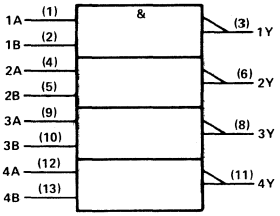
SN54HC00 . . . FH OR FK PACKAGE
SN74HC00 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

Pin numbers shown are for J and N packages.

logic symbol



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC00		74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC02, SN74HC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2684, DECEMBER 1982

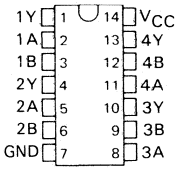
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

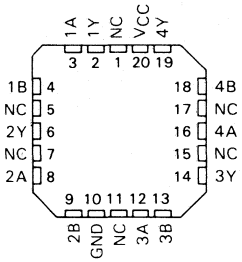
These devices contain four independent 2-input NOR gates. They perform the boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC02 is characterized for operation from −40°C to 85°C.

SN54HC02 . . . J PACKAGE
SN74HC02 . . . J OR N PACKAGE
(TOP VIEW)

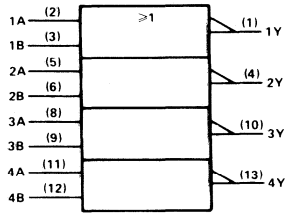


SN54HC02 . . . FH OR FK PACKAGE
SN74HC02 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC02		74HC02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	22 typ	pF

TYPES SN54HC03, SN74HC03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
WITH OPEN-DRAIN OUTPUTS

D2661, APRIL 1982

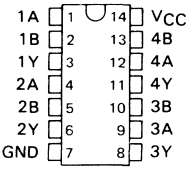
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

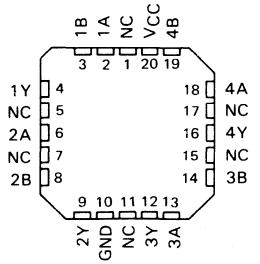
These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. Open-drain devices are often used to generate higher V_{OH} levels.

The SN54HC03 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC03 is characterized for operation from −40°C to 85°C.

SN54HC03 . . . J PACKAGE
SN74HC03 . . . N PACKAGE
(TOP VIEW)



SN54HC03 . . . FH PACKAGE
SN74HC03 . . . FN PACKAGE
(TOP VIEW)



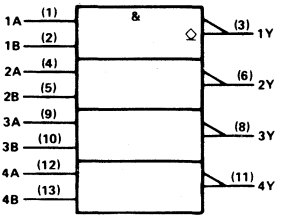
NC – No internal connection

Pin numbers shown are for J and N packages.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol



PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC03		74HC03		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC04, SN74HC04, SN54HCU04, SN74HCU04 HEX INVERTERS

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

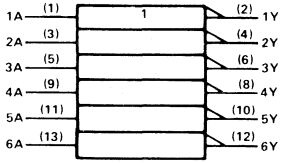
These devices contain six independent inverters. They perform the boolean function Y = $\overline{A}$.

The SN54HC04 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each inverter)

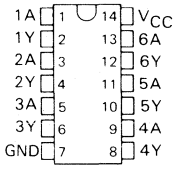
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

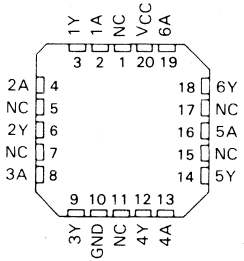


Pin numbers shown are for J and N packages.

SN54HC04 . . . J PACKAGE
SN74HC04 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC04 . . . FH OR FK PACKAGE
SN74HC04 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC04 54HCU04		74HC04 74HCU04		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			85		130		105	ns
			4.5V			17		26		21	
			6.0V			14		22		18	
t_{PHL}			2.0V			85		130		105	
			4.5V			17		26		21	
			6.0V			14		22		18	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC05, SN74HC05
HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

D2661, APRIL 1982

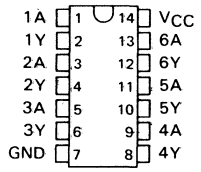
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

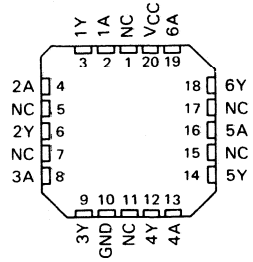
These devices contain six independent inverters. They perform the boolean function $Y = \overline{A}$. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. Open-drain devices are often used to generate higher V_{OH} levels.

The SN54HC05 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC05 is characterized for operation from −40°C to 85°C.

SN54HC05 . . . J PACKAGE
SN74HC05 . . . N PACKAGE
(TOP VIEW)



SN54HC05 . . . FH PACKAGE
SN74HC05 . . . FN PACKAGE
(TOP VIEW)



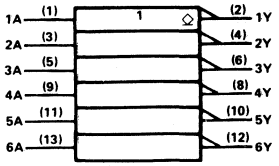
NC – No internal connection

4

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol



Pin numbers shown are for J and N packages.

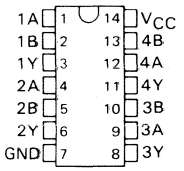
PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC05		74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.0V			115		175		145	ns
			4.5V			23		35		29	
			6.0V			20		30		25	
t_{PHL}			2.0V			85		130		105	
			4.5V			17		26		21	
			6.0V			14		22		18	
t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
C_{pd}	Power dissipation capacitance per inverter at 25°C								20 typ		pF

TYPES SN54HC08, SN74HC08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

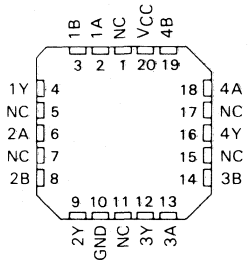
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC08 . . . J PACKAGE
SN74HC08 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC08 . . . FH OR FK PACKAGE
SN74HC08 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

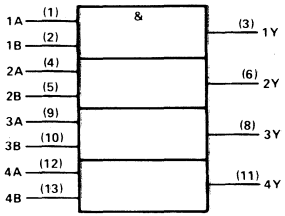
These devices contain four independent 2-input AND gates. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54HC08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC08 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC08		74HC08		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC09, SN74HC09
QUADRUPLE 2-INPUT POSITIVE-AND GATES
WITH OPEN-DRAIN OUTPUTS

D2661, APRIL 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

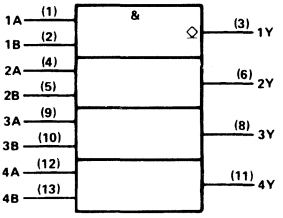
These devices contain four independent 2-input AND gates. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. Open-drain devices are often used to generate higher V_{OH} levels.

The SN54HC09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC09 is characterized for operation from −40°C to 85°C.

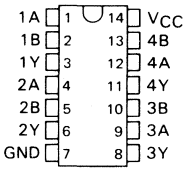
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

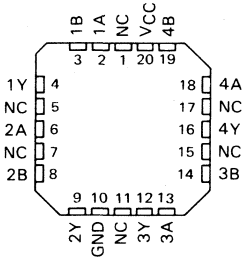
logic symbol



SN54HC09 . . . J PACKAGE
SN74HC09 . . . N PACKAGE
(TOP VIEW)



SN54HC09 . . . FH PACKAGE
SN74HC09 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

Pin numbers shown are for J and N packages.

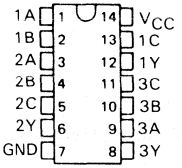
PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC09		74HC09		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A or B	Y	2.0V 4.5V 6.0V			105 25 23		155 36 31		131 31 27	ns
t_{PHL}	A or B	Y	2.0V 4.5V 6.0V			100 20 17		150 30 25		125 25 21	ns
t_r		Y	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
C_{pd}	Power dissipation capacitance per gate at 25°C								20 typ		pF

TYPES SN54HC10, SN74HC10
TRIPLE 3-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC10 . . . J PACKAGE
SN74HC10 . . . J OR N PACKAGE
(TOP VIEW)

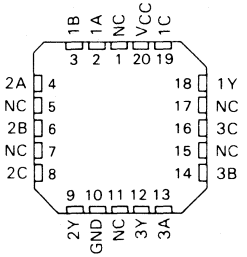


description

These devices contain three independent 3-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \bar{A} + \bar{B} + \bar{C}$ in positive logic.

The SN54HC10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC10 is characterized for operation from −40°C to 85°C.

SN54HC10 . . . FH OR FK PACKAGE
SN74HC10 . . . FH OR FN PACKAGE
(TOP VIEW)

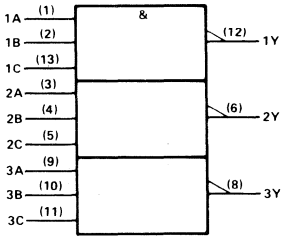


NC — No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC10		74HC10		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC11, SN74HC11
TRIPLE 3-INPUT POSITIVE-AND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

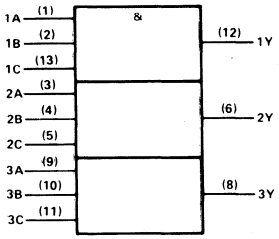
These devices contain three independent 3-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54HC11 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC11 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

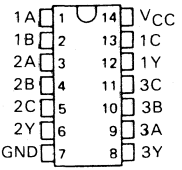
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

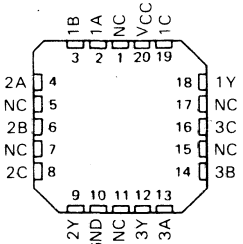


Pin numbers shown are for J and N packages.

SN54HC11 . . . J PACKAGE
SN74HC11 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC11 . . . FH OR FK PACKAGE
SN74HC11 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC11		74HC11		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A, B, or C	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	typ	pF

TYPES SN54HC14, SN74HC14
HEX SCHMITT-TRIGGER INVERTERS

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

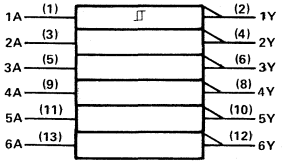
These Schmitt-trigger devices contain six independent inverters. They perform the boolean function Y = A.

The SN54HC14 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC14 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

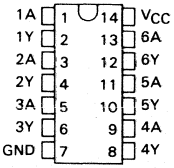
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

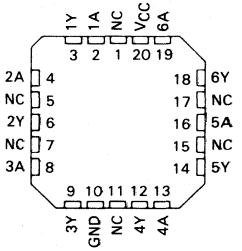


Pin numbers shown are for J and N packages.

SN54HC14 . . . J PACKAGE
SN74HC14 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC14 . . . FH OR FK PACKAGE
SN74HC14 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC14		74HC14		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	A	Y	2.0V			140		210		175	ns
			4.5V			28		42		35	
			6.0V			24		36		30	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	typ	pF

PRODUCT PREVIEW

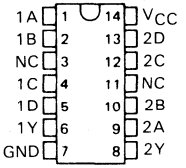
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC20, SN74HC20
DUAL 4-INPUT POSITIVE-NAND GATES

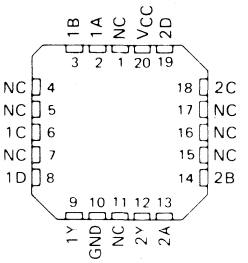
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC20 . . . J PACKAGE
SN74HC20 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC20 . . . FH OR FK PACKAGE
SN74HC20 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

Pin numbers shown are for J and N packages.

description

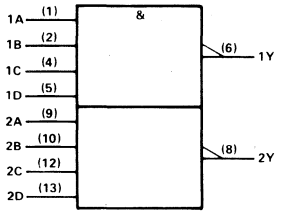
These devices contain two independent 4-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54HC20 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC20 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC20		74HC20		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C, or, D	Y	2.0V			110		165		140	ns
			4.5V			22		33		28	
			6.0V			19		28		24	
t_{PHL}			2.0V			110		165		140	
			4.5V			22		33		28	
			6.0V			19		28		24	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	25 typ	pF

TYPES SN54HC21, SN74HC21
DUAL 4-INPUT POSITIVE-AND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

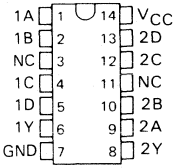
These devices contain two independent 4-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$ in positive logic.

The SN54HC21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC21 is characterized for operation from −40°C to 85°C.

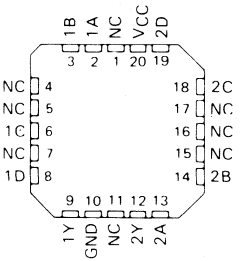
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

SN54HC21 . . . J PACKAGE
SN74HC21 . . . J OR N PACKAGE
(TOP VIEW)

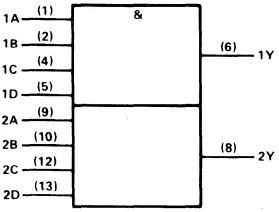


SN54HC21 . . . FH OR FK PACKAGE
SN74HC21 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC21		74HC21		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C, or D	Y	2.0V			110		165		140	ns
			4.5V			22		33		28	
			6.0V			19		28		24	
t_{PHL}			2.0V			110		165		140	
			4.5V			22		33		28	
			6.0V			19		28		24	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	25 typ	pF

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC27, SN74HC27 TRIPLE 3-INPUT POSITIVE-NOR GATES

D2684, DECEMBER 1982

Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

description

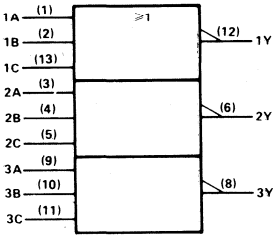
These devices contain three independent 3-input NOR gates. They perform the boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54HC27 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC27 is characterized for operation from -40°C to 85°C.

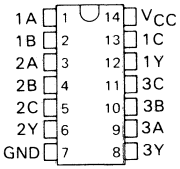
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

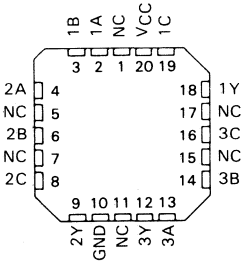
logic symbol



SN54HC27 . . . J PACKAGE
SN74HC27 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC27 . . . FH OR FK PACKAGE
SN74HC27 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC27		74HC27		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	
C_{pd}	Power dissipation capacitance per gate at 25°C								25 typ		pF

TYPES SN54HC30, SN74HC30
8-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following boolean functions in positive logic:

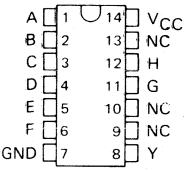
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

or

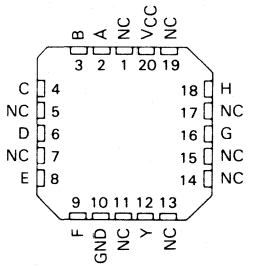
$$Y = \bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F} + \bar{G} + \bar{H}$$

The SN54HC30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC30 is characterized for operation from −40°C to 85°C.

SN54HC30 . . . J PACKAGE
SN74HC30 . . . J OR N PACKAGE
(TOP VIEW)

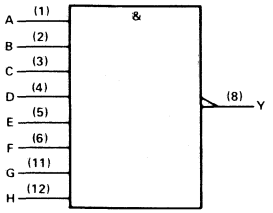


SN54HC30 . . . FH OR FK PACKAGE
SN74HC30 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC30		74HC30		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	A thru H	Y	2.0V 4.5V 6.0V			100 20 17		150 30 25		125 25 21	ns
t_r, t_f		Y	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

PRODUCT PREVIEW

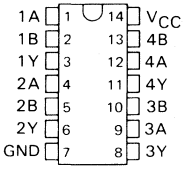
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC32, SN74HC32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

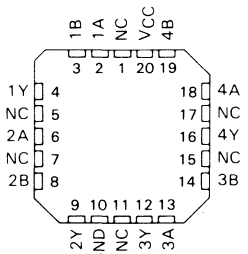
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC32 . . . J PACKAGE
SN74HC32 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC32 . . . FH OR FK PACKAGE
SN74HC32 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

Pin numbers shown are for J and N packages.

description

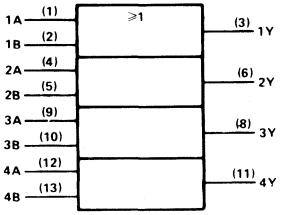
These devices contain four independent 2-input OR gates. They perform the boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54HC32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC32 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC32		74HC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC36, SN74HC36
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2684, DECEMBER 1982

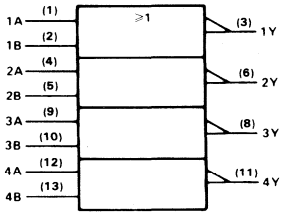
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input NOR gates. They perform the boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

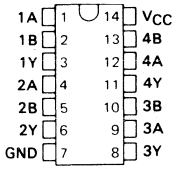
The SN54HC36 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC36 is characterized for operation from −40°C to 85°C.

logic symbol

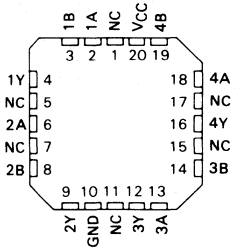


Pin numbers shown are for J and N packages.

SN54HC36 . . . J PACKAGE
SN74HC36 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC36 . . . FH OR FK PACKAGE
SN74HC36 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC36		74HC36		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	20 typ	pF

TYPES SN54HC42, SN74HC42
4-LINE TO 10-LINE DECODERS (1-of-10)

D2684, DECEMBER 1982

- **Full Decoding of Input Logic**
- **All Outputs Are Off for Invalid BCD Conditions**
- **Also for Application as 3-Line to 8-Line Decoders**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

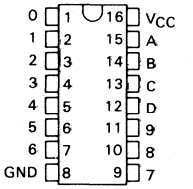
These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

The SN54HC42 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC42 is characterized for operation from −40°C to 85°C.

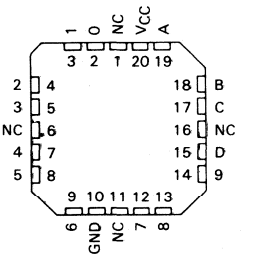
FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

SN54HC42 . . . J PACKAGE
SN74HC42 . . . J OR N PACKAGE
(TOP VIEW)

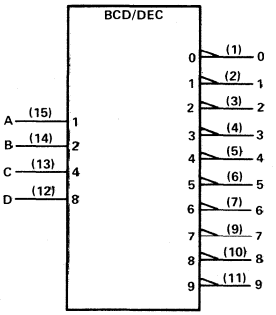


SN54HC42 . . . FH OR FK PACKAGE
SN74HC42 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC42		74HC42		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A,B, C, or D	0 thru 9	2.0V			150		225		190	ns
			4.5V			30		45		38	
			6.0V			26		38		32	
t_{PHL}			2.0V			150		225		190	
			4.5V			30		45		38	
			6.0V			26		38		32	
t_r		ANY	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	39 typ	pF

TYPES SN54HC51, SN74HC51 AND-OR-INVERT GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

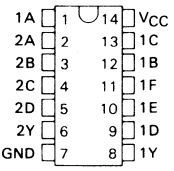
The 'HC51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The device performs the following boolean functions:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

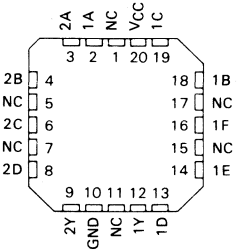
$$2Y = \overline{(2A \cdot 2B \cdot) + (2C \cdot 2D)}$$

The SN54HC51 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC51 is characterized for operation from −40°C to 85°C.

SN54HC51 . . . J PACKAGE
SN74HC51 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC51 . . . FH OR FK PACKAGE
SN74HC51 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

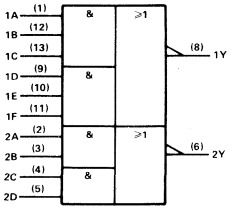
FUNCTION TABLES

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

Pin numbers shown are for J and N packages.

logic symbol



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC51		74HC51		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	ANY	Y	2.0V			140		210		175	ns
			4.5V			28		42		35	
			6.0V			24		36		30	
t_{PHL}			2.0V			140		210		175	
			4.5V			28		42		35	
			6.0V			24		36		30	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	typ	pF

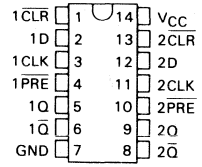
PRODUCT PREVIEW

TYPES SN54HC74, SN74HC74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

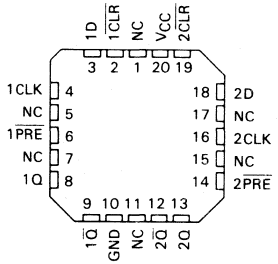
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC74 . . . J PACKAGE
SN74HC74 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC74 . . . FH OR FK PACKAGE
SN74HC74 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high) data at the D input meeting the setup time requirements are transferred to the outputs on the the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

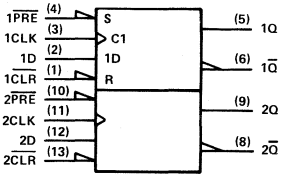
The SN54HC74 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC74 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	Q_0

†This configuration is nonstable; that is, it will not persist when Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC74			74HC74			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		3	0		4	MHz
		4.5V	0		16	0		20	
		6.0V	0		19	0		23	
t_w	PRE or CLR low	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	CLK high	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
	CLK low	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_{su}	Data	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	PRE or CLR inactive	2.0V	185			160			
		4.5V	37			32			
		6.0V	31			27			
t_h		2.0V	0			0			ns
		4.5V	0			0			
		6.0V	0			0			

4

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC74		74HC74		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V	5			3		4		MHz
			4.5V	25			16		20		
			6.0 V	29			19		23		
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	2.0V			230		345		290	ns
			4.5V			46		69		58	
			6.0V			39		59		49	
t_{PHL}			2.0V			230		345		290	
			4.5V			46		69		58	
			6.0V			39		59		49	
t_{PLH}	CLK	Q or $\overline{Q}$	2.0V			175		250		220	ns
			4.5V			35		50		44	
			6.0V			30		42		37	
t_{PHL}			2.0V			175		250		220	
			4.5V			35		50		44	
			6.0V			30		42		37	
t_{PLH}		Q or $\overline{Q}$	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_{PHL}			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

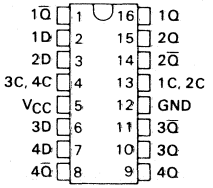
C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

TYPES SN54HC75, SN74HC75
4-BIT BISTABLE LATCHES

D2684, DECEMBER 1982

- **Complementary Q and $\overline{Q}$ Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC75 . . . J PACKAGE
SN74HC75 . . . J OR N PACKAGE
(TOP VIEW)



For chip carrier information, contact the factory

4

description

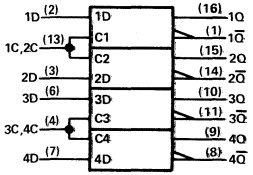
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The SN54HC75 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC75 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC75			74HC75			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	2.0V 4.5V 6.0V							ns
t_{su}	2.0V 4.5V 6.0V			195 39 33			165 33 28	ns
t_h	2.0V 4.5V 6.0V			90 18 15			75 15 13	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC75		74HC75		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2.0V 4.5V 6.0V								ns
t_{pd}	D	$\overline{Q}$	2.0V 4.5V 6.0V			190 38 32		285 57 48		240 48 41	ns
t_{pd}	C	Q	2.0V 4.5V 6.0V			145 29 25		220 44 37		181 36 31	ns
t_{pd}	C	$\overline{Q}$	2.0V 4.5V 6.0V			145 29 25		220 44 37		181 36 31	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

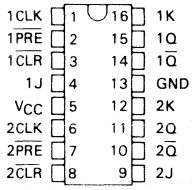
C_{pd}	Power dissipation capacitance per latch at 25°C	typ	pF

TYPES SN54HC76, SN74HC76
DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC76 . . . J PACKAGE
SN74HC76 . . . J OR N PACKAGE
(TOP VIEW)



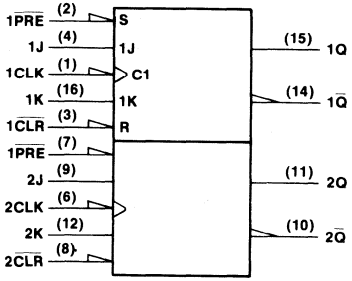
For chip carrier information, contact the factory.

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can also perform as toggle flip-flops by tying J and K high.

The SN54HC76 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC76 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC76			74HC76			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		3	0		4	MHz
		4.5V	0		16	0		20	
		6.0V	0		19	0		23	
t_w	PRE or CLR low	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	CLK high	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
	CLK low	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_{su}	Data	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	PRE or CLR inactive	2.0V	185			160			
		4.5V	37			32			
		6.0V	31			27			
t_h		2.0V	0			0			ns
		4.5V	0			0			
		6.0V	0			0			

4

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC76		74HC76		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V	5			3		4		MHz
			4.5V	25			16		20		
			6.0 V	29			19		23		
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	2.0V			230		345		290	ns
			4.5V			46		69		58	
			6.0V			39		59		49	
t_{PHL}			2.0V			230		345		290	
			4.5V			46		69		58	
			6.0V			39		59		49	
t_{PLH}	CLK	Q or $\overline{Q}$	2.0V			175		250		220	ns
			4.5V			35		50		44	
			6.0V			30		42		37	
t_{PHL}			2.0V			175		250		220	
			4.5V			35		50		44	
			6.0V			30		42		37	
t_r		Q or $\overline{Q}$	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

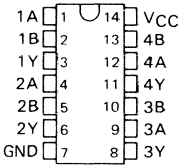
C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

TYPES SN54HC86, SN74HC86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

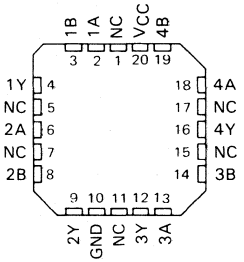
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC86 . . . J PACKAGE
SN74HC86 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC86 . . . FH OR FK PACKAGE
SN74HC86 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

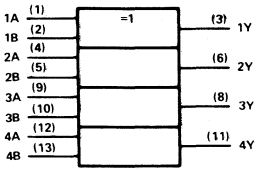
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC86 is characterized for operation from −40°C to 85°C.

logic symbol



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Pin numbers shown are for J and N packages.

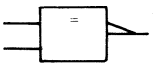
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

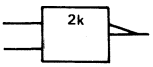
These are five equivalent Exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



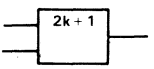
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC86		74HC86		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	A or B	Y	2.0V 4.5V 6.0V			100 20 17		150 30 25		125 25 21	ns
t_r, t_f		Y	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
C_{pd}	Power dissipation capacitance per gate at 25°C							40 typ			pF

4

TYPES SN54HC107, SN74HC107
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

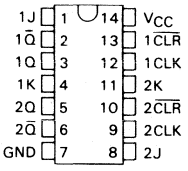
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

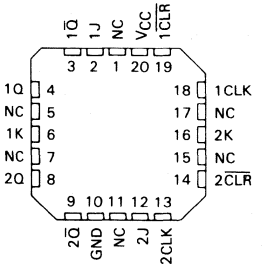
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC107 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC107 is characterized for operation from −40°C to 85°C.

SN54HC107 . . . J PACKAGE
SN74HC107 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC107 . . . FH OR FK PACKAGE
SN74HC107 . . . FH OR FN PACKAGE
(TOP VIEW)

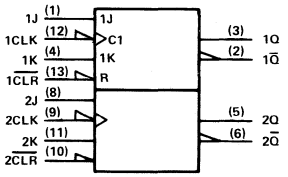


NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC107			74HC107			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V	0 0 0		3 16 19	0 0 0		4 20 23	MHz
t_w	$\overline{CLR}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data (J,K)	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	$\overline{CLR}$ Inactive	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

4

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC107		74HC107		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH} t_{PHL}	$\overline{CLR}$	Q, $\overline{Q}$	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PLH} t_{PHL}	CLK	Q, $\overline{Q}$	2.0V 4.5V 6.0V			175 35 30		265 53 45		220 44 37	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	typ	pF

TYPES SN54HC109, SN74HC109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2684, DECEMBER 1982

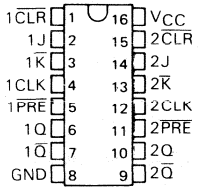
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

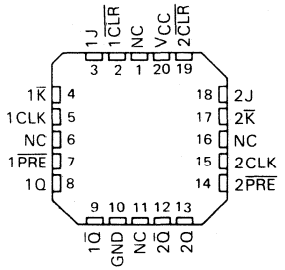
These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The SN54HC109 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC109 is characterized for operation from -40°C to 85°C.

SN54HC109 . . . J PACKAGE
SN74HC109 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC109 . . . FH OR FK PACKAGE
SN74HC109 . . . FH OR FN PACKAGE
(TOP VIEW)



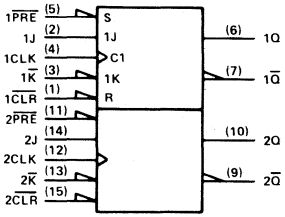
NC — No Internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when Preset or Clear return to their inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC109			74HC109			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	PRE or CLR low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data (J,K)	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	PRE or CLR inactive	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_h	JEDEC SAID 5 ns	2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC109		74HC109		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}	PRE or CLR	Q or Q BAR	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PHL}			2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	
t_{PLH}	CLK	Q or Q BAR	2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	ns
t_{PHL}			2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	
t_r		Q or Q BAR	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
t_f			2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	

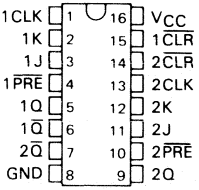
C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

TYPES SN54HC112, SN74HC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

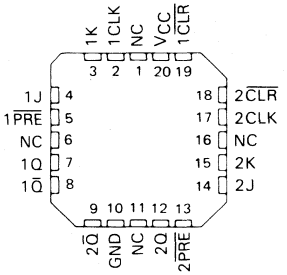
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC112 . . . J PACKAGE
SN74HC112 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC112 . . . FH OR FK PACKAGE
SN74HC112 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

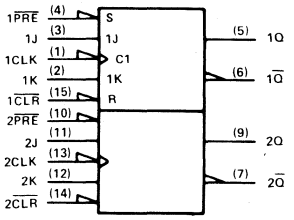
The SN54HC112 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC112 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC112			74HC112			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	PRE or CLR low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	PRE or CLR inactive	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

4

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC112		74HC112		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0 V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PHL}			2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	
t_{PLH}	CLK	Q or $\overline{Q}$	2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	ns
t_{PHL}			2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	
t_r		Q or $\overline{Q}$	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
t_f			2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

TYPES SN54HC113, SN74HC113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2684, DECEMBER 1982

Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

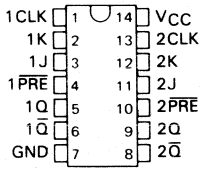
Dependable Texas Instruments Quality and Reliability

description

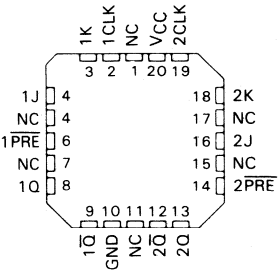
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC113 is characterized for operation from −40°C to 85°C.

SN54HC113 . . . J PACKAGE
SN74HC113 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC113 . . . FH OR FK PACKAGE
SN74HC113 . . . FH OR FN PACKAGE
(TOP VIEW)

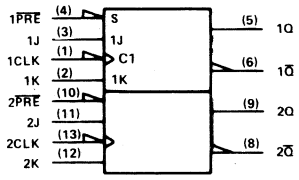


NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC113			74HC113			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	PRE low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	PRE inactive	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC113		74HC113		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0 V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}	PRE	Q or $\overline{Q}$	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PHL}			2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	
t_{PLH}	CLK	Q or $\overline{Q}$	2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	ns
t_{PHL}			2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	
t_r		Q or $\overline{Q}$	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
t_f			2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

HIGH-SPEED CMOS LOGIC

TYPES SN54HC114, SN74HC114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2684, DECEMBER 1982

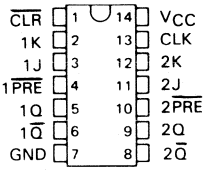
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

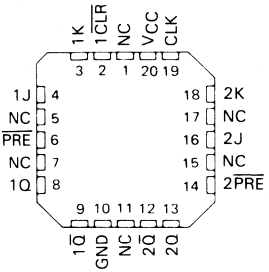
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC114 is characterized for operation from −40°C to 85°C.

SN54HC114 . . . J PACKAGE
SN74HC114 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC114 . . . FH OR FK PACKAGE
SN74HC114 . . . FH OR FN PACKAGE
(TOP VIEW)



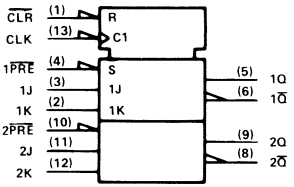
NC — No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC114			74HC114			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	PRE or CLR	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	PRE or CLR inactive	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC114		74HC114		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0 V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PHL}			2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	
t_{PLH}	CLK	Q or $\overline{Q}$	2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	ns
t_{PHL}			2.0V 4.5V 6.0V			175 35 30		250 50 42		220 44 37	
t_r		Q or $\overline{Q}$	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
t_f			2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	35 typ	pF

TYPES SN54HC133, SN74HC133
13-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

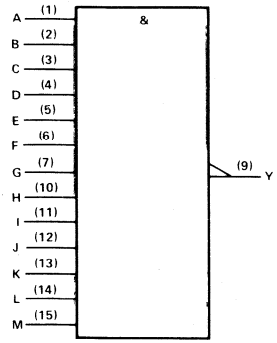
These devices contain a single 13-input NAND gate. They perform the boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

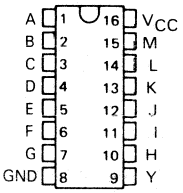
The SN54HC133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC133 is characterized for operation from −40°C to 85°C.

logic symbol

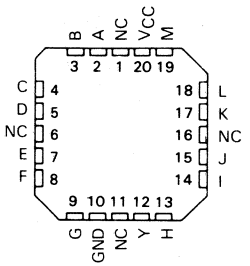


Pin numbers shown are for J and N packages.

SN54HC133 . . . J PACKAGE
SN74HC133 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC133 . . . FH OR FK PACKAGE
SN74HC133 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC133		74HC133		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	ANY	Y	2.0V			150		225		190	ns
			4.5V			30		45		38	
			6.0V			26		38		33	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance at 25°C	typ	pF

PRODUCT PREVIEW

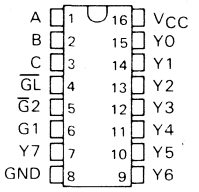
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC137, SN74HC137, SN54HCT137, SN74HCT137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

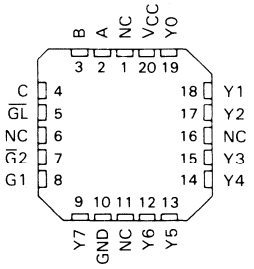
D2684, DECEMBER 1982

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC137 . . . J PACKAGE
SN74HC137 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC137 . . . FH OR FK PACKAGE
SN74HC137 . . . FH OR FN PACKAGE
(TOP VIEW)



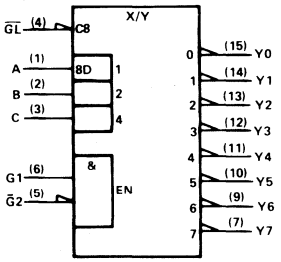
NC — No internal connection

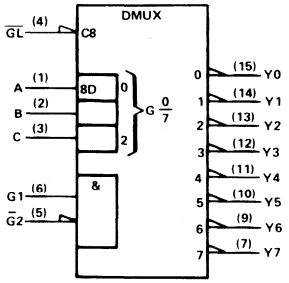
description

The 'HC137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HC137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HC137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HC137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC137 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC137 54HCT137			74HC137 74HCT137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	2.0V 4.5V 6.0V	0 0 0		3 16 19	0 0 0		4 20 23	MHz
t_w	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_h	2.0V 4.5V 6.0V							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC137 54HCT137		74HC137 74HCT137		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{pd}	A, B, C	Y	2.0V 4.5V 6.0V			215 43 37		325 65 55		270 54 46	ns
t_{pd}	$\overline{G2}$	Y	2.0V 4.5V 6.0V			205 41 35		310 62 53		255 51 43	ns
t_{pd}	G1	Y	2.0V 4.5V 6.0V			195 39 33		295 59 50		245 49 42	ns
t_{pd}	$\overline{GL}$	Y	2.0V 4.5V 6.0V			210 42 36		315 63 54		265 53 45	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

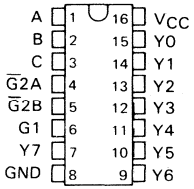
C_{pd}	Power dissipation capacitance at 25°C	60 typ	pF

TYPES SN54HC138, SN74HC138, SN54HCT138, SN74HCT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

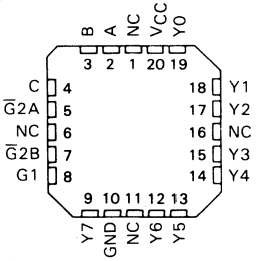
D2684, DECEMBER 1982

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC138 . . . J PACKAGE
SN74HC138 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC138 . . . FH OR FK PACKAGE
SN74HC138 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

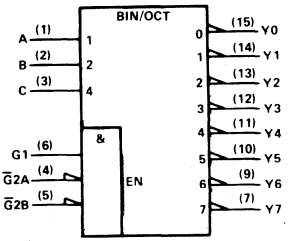
description

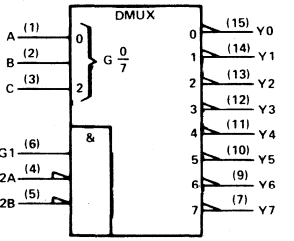
The 'HC138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54HC138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC138 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2}$ $\overline{G2A}$ - $\overline{G2B}$

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC138 54HCT138		74HC138 74HCT138		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	ANY	2.0V			225		335		285	ns
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PHL}	B, or C	ANY	2.0V			225		335		285	ns
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PLH}	ENAB.	ANY	2.0V			225		335		285	ns
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PHL}			2.0V			225		335		285	
			4.5V			45		67		57	
			6.0V			38		57		48	
t_r		ANY	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance at 25°C	40 typ	pF

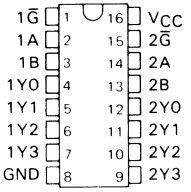
TYPES SN54HC139, SN74HC139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

D2684, DECEMBER 1982

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

Dependable Texas Instruments Quality and Reliability

SN54HC139 . . . J PACKAGE
SN74HC139 . . . J OR N PACKAGE
(TOP VIEW)



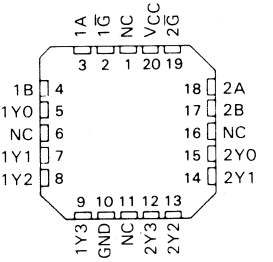
description

The 'HC139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The 'HC139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

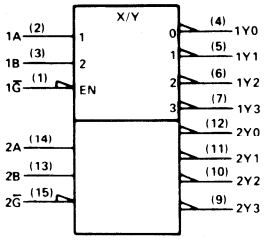
The SN54HC139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC139 is characterized for operation from −40°C to 85°C.

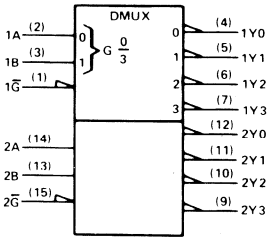
SN54HC139 . . . FH OR FK PACKAGE
SN74HC139 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC139		74HC139		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.0V			225		335		285	ns
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PHL}			2.0V			225		335		285	
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PLH}	$\overline{G}$	Y	2.0V			225		335		285	ns
			4.5V			45		67		57	
			6.0V			38		57		48	
t_{PHL}			2.0V			225		335		285	
			4.5V			45		67		57	
			6.0V			38		57		48	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance at 25°C	26 typ	pF

TYPES SN54HC151, SN74HC151
DATA SELECTORS/MULTIPLEXERS

D2684, DECEMBER 1982

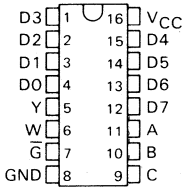
- **3-Line to 1-Line Multiplexers Can Perform As:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

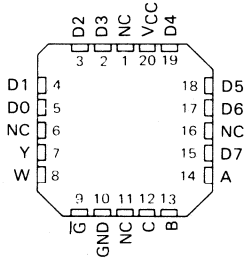
These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54HC151 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC151 is characterized for operation from −40°C to 85°C.

SN54HC151 . . . J PACKAGE
SN74HC151 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC151 . . . FH OR FK PACKAGE
SN74HC151 . . . FH OR FN PACKAGE
(TOP VIEW)



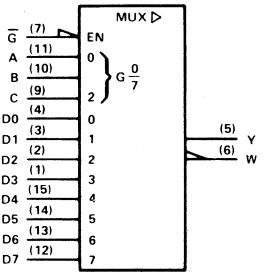
NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC151		74HC151		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A, B, or C	Y	50 pF	2.0V			205		310		255	ns
			150 pF	2.0V			290		440		360	
			50 pF	4.5V			41		62		51	
			150 pF	4.5V			58		88		72	
			50 pF	6.0V			35		53		43	
			150 pF	6.0V			50		75		62	
t_{PLH}, t_{PHL}	A, B, or C	W	50 pF	2.0V			205		310		255	ns
			150 pF	2.0V			290		440		360	
			50 pF	4.5V			41		62		51	
			150 pF	4.5V			58		88		72	
			50 pF	6.0V			35		53		43	
			150 pF	6.0V			50		75		62	
t_{PLH}, t_{PHL}	ANY D	Y	50 pF	2.0V			170		255		213	ns
			150 pF	2.0V			225		385		318	
			50 pF	4.5V			34		51		43	
			150 pF	4.5V			51		77		64	
			50 pF	6.0V			29		44		36	
			150 pF	6.0V			44		66		55	
t_{PLH}, t_{PHL}	ANY D	W	50 pF	2.0V			170		255		213	ns
			150 pF	2.0V			225		385		318	
			50 pF	4.5V			34		51		43	
			150 pF	4.5V			51		77		64	
			50 pF	6.0V			29		44		36	
			150 pF	6.0V			44		66		55	
t_{PLH}, t_{PHL}	$\overline{G}$	Y	50 pF	2.0V			135		205		169	ns
			150 pF	2.0V			220		335		274	
			50 pF	4.5V			27		41		34	
			150 pF	4.5V			44		67		55	
			50 pF	6.0V			23		35		29	
			150 pF	6.0V			38		57		48	
t_{PLH}, t_{PHL}	$\overline{G}$	W	50 pF	2.0V			135		205		169	ns
			150 pF	2.0V			220		335		274	
			50 pF	4.5V			27		41		34	
			150 pF	4.5V			44		67		55	
			50 pF	6.0V			23		35		29	
			150 pF	6.0V			38		57		48	
t_r, t_f			50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance at 25°C	100 typ	pF

4

TYPES SN54HC152, SN74HC152
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

D2684, DECEMBER 1982

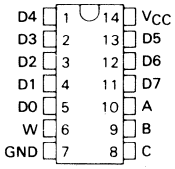
- **Selects One-of-Eight Data Sources**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

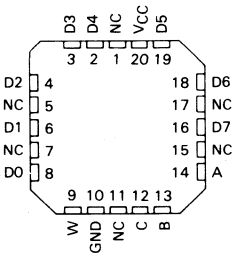
These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired one-of-eight data sources.

The SN54HC152 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC152 is characterized for operation from −40°C to 85°C.

SN54HC152 . . . J PACKAGE
SN74HC152 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC152 . . . FH OR FK PACKAGE
SN74HC152 . . . FH OR FN PACKAGE
(TOP VIEW)

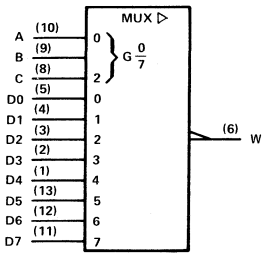


NC — No internal connection

FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC152		74HC152		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A, B, or C	W	50 pF	2.0V			170		255		213	ns
			150 pF	2.0V			225		385		318	
			50 pF	4.5V			34		51		43	
			150 pF	4.5V			51		77		64	
			50 pF	6.0V			29		44		36	
			150 pF	6.0V			44		66		55	
t_{PLH}, t_{PHL}	ANY D	W	50 pF	2.0V			130		195		163	ns
			150 pF	2.0V			215		325		268	
			50 pF	4.5V			26		39		33	
			150 pF	4.5V			43		65		54	
			50 pF	6.0V			22		33		28	
			150 pF	6.0V			37		55		47	
t_r, t_f			50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per latch at 25°C	100 typ	pF

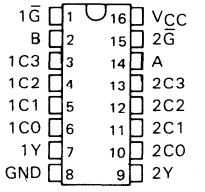
4

TYPES SN54HC153, SN74HC153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

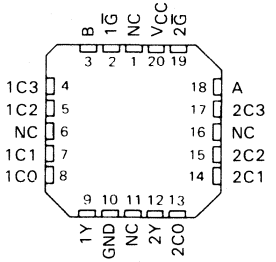
D2684, DECEMBER 1982

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC153 . . . J PACKAGE
SN74HC153 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC153 . . . FH OR FK PACKAGE
SN74HC153 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

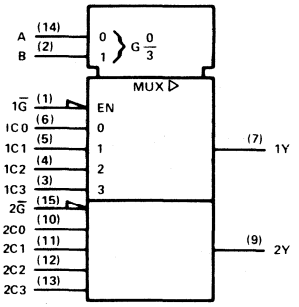
The SN54HC153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC153 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC153		74HC153		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PHL}			50 pF	2.0V			150		225		190	
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PLH}	DATA (ANY C)	Y	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PHL}			50 pF	2.0V			150		225		190	
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PLH}	G	Y	50 pF	2.0V			100		150		125	ns
			150 pF	2.0V			185		280		230	
			50 pF	4.5V			20		30		25	
			150 pF	4.5V			37		56		46	
			50 pF	6.0V			17		26		21	
			150 pF	6.0V			32		48		40	
t_{PHL}			50 pF	2.0V			100		150		125	
			150 pF	2.0V			185		280		230	
			50 pF	4.5V			20		30		25	
			150 pF	4.5V			37		56		46	
			50 pF	6.0V			17		26		21	
			150 pF	6.0V			32		48		40	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per mux. at 25°C	typ	pF

HIGH-SPEED CMOS LOGIC

TYPES SN54HC157, SN54HC158, SN74HC157, SN74HC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

D2684, DECEMBER 1982

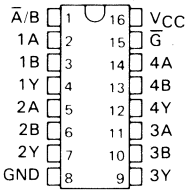
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

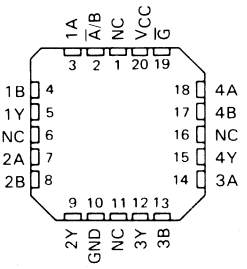
These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'HC157 presents true data whereas the 'HC158 presents inverted data.

The SN54HC157 and SN54HC158 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC157 and SN74HC158 are characterized for operation from −40°C to 85°C.

SN54HC157, SN54HC158 . . . J PACKAGE
SN74HC157, SN74HC158 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC157, SN54HC158 . . . FH OR FK PACKAGE
SN74HC157, SN74HC158 . . . FH OR FN PACKAGE
(TOP VIEW)



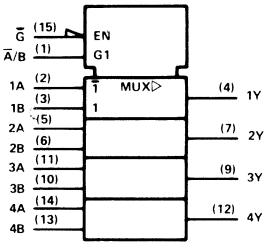
NC — No internal connection

FUNCTION TABLE

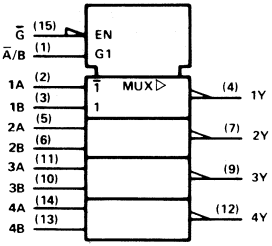
INPUTS				OUTPUT Y	
STROBE $\overline{G}$	SELECT $\overline{A}/B$	DATA A	DATA B	'HC157	'HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic symbols

'HC157



'HC158



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

'HC157 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC157		74HC157		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PLH}	$\overline{A}$/B	Y	50 pF	2.0V			125		190		155	ns
			150 pF	2.0V			210		320		260	
			50 pF	4.5V			25		38		31	
			150 pF	4.5V			42		64		52	
			50 pF	6.0V			21		32		26	
			150 pF	6.0V			36		54		45	
t_{PHL}			50 pF	2.0V			125		190		155	
			150 pF	2.0V			210		320		260	
			50 pF	4.5V			25		38		31	
			150 pF	4.5V			42		64		52	
			50 pF	6.0V			21		32		26	
			150 pF	6.0V			36		54		45	
t_{PLH}	$\overline{G}$	Y	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per MUX, at 25°C	typ	pF

'HC158 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC158		74HC158		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PLH}	$\overline{A}$/B	Y	50 pF	2.0V			110		165		140	ns
			150 pF	2.0V			195		295		245	
			50 pF	4.5V			22		33		28	
			150 pF	4.5V			39		59		49	
			50 pF	6.0V			19		28		24	
			150 pF	6.0V			34		50		43	
t_{PHL}			50 pF	2.0V			110		165		140	
			150 pF	2.0V			195		295		245	
			50 pF	4.5V			22		33		28	
			150 pF	4.5V			39		59		49	
			50 pF	6.0V			19		28		24	
			150 pF	6.0V			34		50		43	
t_{PLH}	$\overline{G}$	Y	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

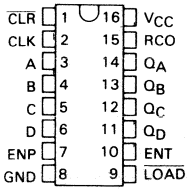
C_{pd}	Power dissipation capacitance per MUX, at 25°C	typ	pF

TYPES SN54HC160 THRU SN54HC163, SN74HC160 THRU SN74HC163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

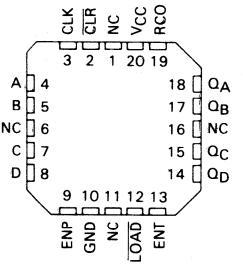
D2684, DECEMBER 1982

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC'. . . J PACKAGE
SN74HC'. . . J or N PACKAGE
(TOP VIEW)



SN54HC' . . . FH or FK PACKAGE
SN74HC' . . . FH or FN PACKAGE
(TOP VIEW)



NC — no internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC160 and 'HC162 are decade counters, and the 'HC161 and 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'HC160 and 'HC161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'HC162 and 'HC163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

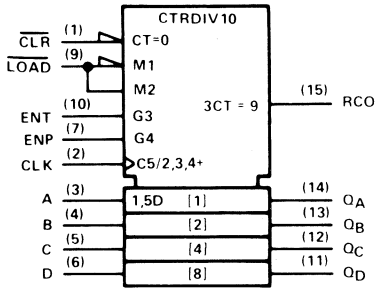
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

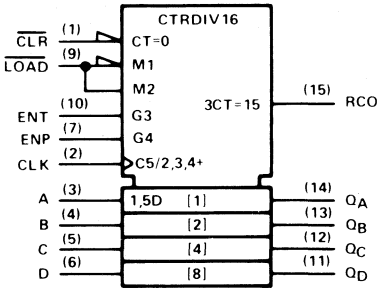
The SN54HC160 through SN54HC163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC160 through SN74HC163 are characterized for operation from −40°C to 85°C.

logic symbols

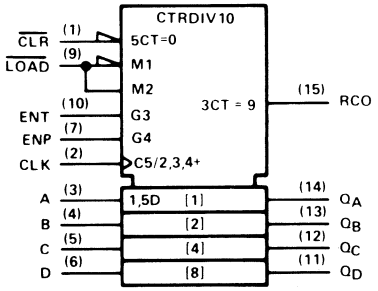
HC160 DECADE COUNTER
WITH DIRECT CLEAR



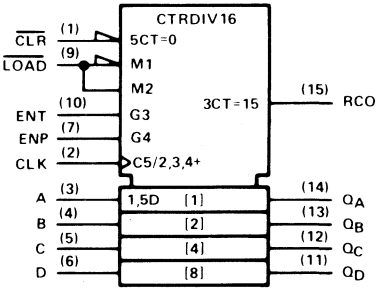
'HC161 BINARY COUNTER
WITH DIRECT CLEAR



'HC162 DECADE COUNTER
WITH SYNCHRONOUS CLEAR



'HC163 BINARY COUNTER
WITH SYNCHRONOUS CLEAR

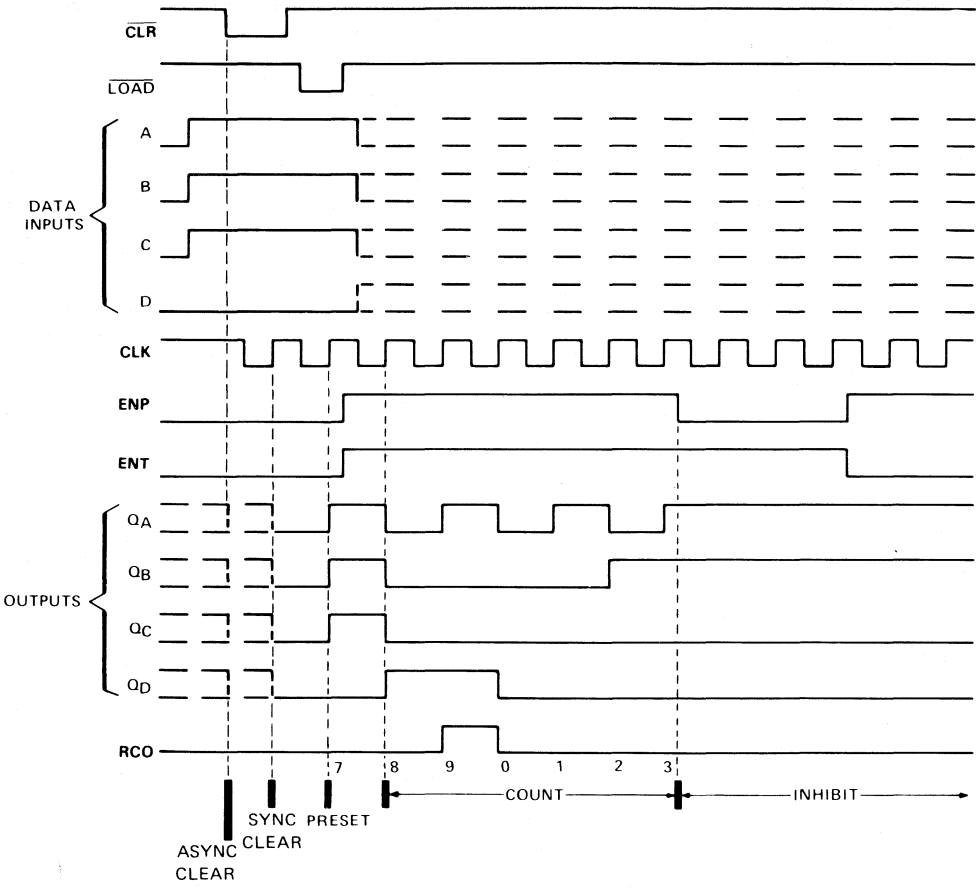


Pin numbers shown are for J and N packages.

'160 and '162 output sequence

Illustrated below is the following sequence:

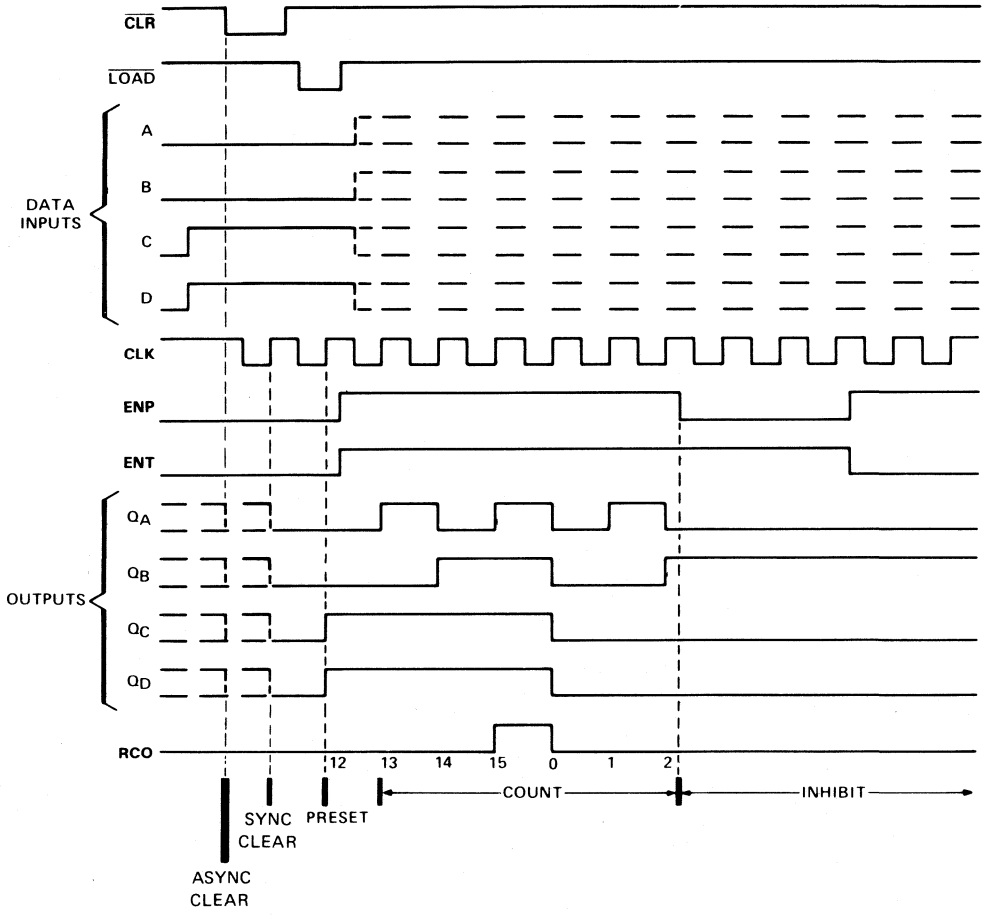
1. Clear outputs to zero (SN54HC160 and SN74HC160 are asynchronous; SN54HC162 and SN74HC162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



'161 and '163 output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC161 and SN74HC161 are asynchronous; SN54HC163 and SN74HC163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit



timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC160 54HC161			74HC160 74HC161			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		3	0		4	MHz
		4.5V	0		16	0		20	
		6.0V	0		19	0		23	
t_w	CLK high or low	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	$\overline{CLR}$ low	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_{su}	A, B, C, or D	2.0V	225			190			ns
		4.5V	45			38			
		6.0V	38			37			
	ENP, ENT	2.0V	255			215			
		4.5V	51			43			
		6.0V	43			37			
	$\overline{CLR}$ Inactive	2.0V	190			155			
		4.5V	38			31			
		6.0V	32			26			
	$\overline{LOAD}$ low	2.0V	205			170			
		4.5V	41			34			
		6.0V	35			29			
t_h		2.0V	0			0			ns
		4.5V	0			0			
		6.0V	0			0			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC160 54HC161		74HC160 74HC161		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V	5			3		4		MHz
			4.5V	25			16		20		
			6.0V	29			19		23		
t_{PLH}, t_{PHL}	CLK	RCO	2.0V			215		325		270	ns
			4.5V			43		65		54	
			6.0V			37		55		46	
t_{PLH}, t_{PHL}	CLK	ANY Q	2.0V			205		310		255	ns
			4.5V			41		62		51	
			6.0V			35		53		43	
t_{PLH}, t_{PHL}	ENT	RCO	2.0V			195		295		245	ns
			4.5V			39		59		49	
			6.0V			33		50		42	
t_{PHL}	$\overline{CLR}$	ANY Q	2.0V			210		315		265	ns
			4.5V			42		63		53	
			6.0V			36		54		45	
t_{PHL}	$\overline{CLR}$	RCO	2.0V			220		330		275	ns
			4.5V			44		66		55	
			6.0V			37		56		47	
t_r, t_f		ANY	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
C_{pd}	Power dissipation capacitance at 25°C								60 typ		pF

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC162 54HC163			74HC162 74HC163			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V	0 0 0		3 16 19	0 0 0		4 20 23	MHz
t_w	CLK high or low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	A, B, C, or D	2.0V 4.5V 6.0V	225 45 38			190 38 32			ns
	ENP, ENT	2.0V 4.5V 6.0V	255 51 43			215 43 37			
	$\overline{CLR}$ low	2.0V 4.5V 6.0V	240 48 41			200 40 34			
	$\overline{CLR}$ high (Inactive)	2.0V 4.5V 6.0V	240 48 41			200 40 34			
	$\overline{LOAD}$ low	2.0V 4.5V 6.0V	205 41 35			170 34 29			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

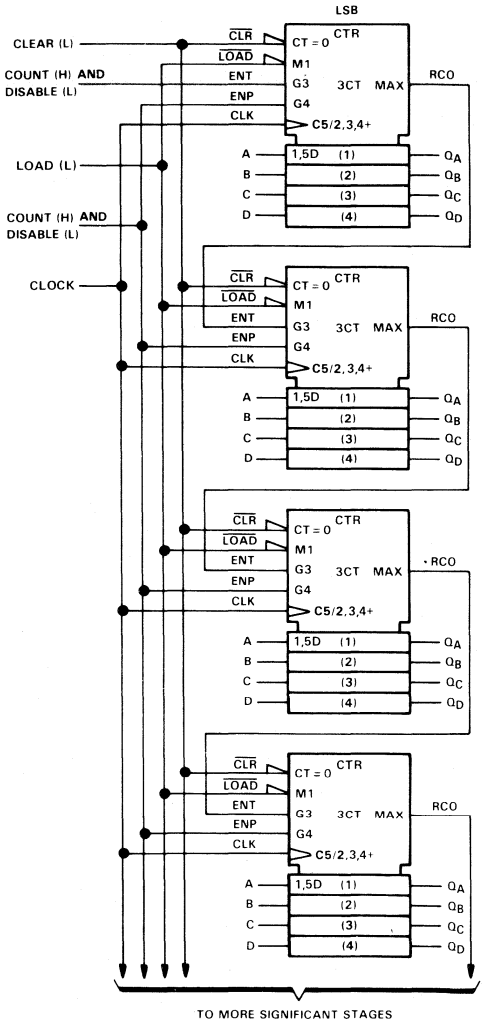
PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF						UNIT
				T_A = 25°C			54HC162 54HC163		74HC162 74HC163	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	CLK	RCO	2.0V 4.5V 6.0V			215 43 37		325 65 55		270 54 46	ns
t_{PLH}, t_{PHL}	CLK	ANY Q	2.0V 4.5V 6.0V			205 41 35		310 62 53		255 51 43	ns
t_{PLH}, t_{PHL}	ENT	RCO	2.0V 4.5V 6.0V			195 39 33		295 59 50		245 49 42	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance at 25°C	60 typ	pF

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC160 and 'HC162 will count in BCD, and the 'HC161 and 'HC163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

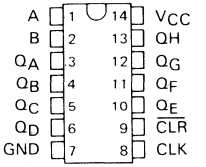


TYPES SN54HC164, SN74HC164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

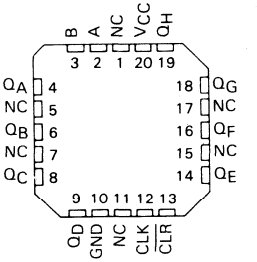
D2684, DECEMBER 1982

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC164 . . . J PACKAGE
SN74HC164 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC164 . . . FH OR FK PACKAGE
SN74HC164 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

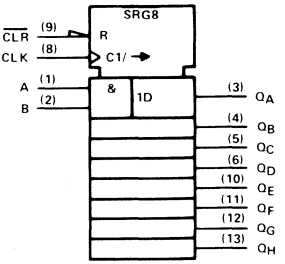
The SN54HC164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC164 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H high level (steady state), L low level (steady state)
X irrelevant (any input, including transitions)
↑ transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Gn} the level of Q_A or Q_G before the most recent ↑ transition of the clock, indicates a one bit shift

logic symbol



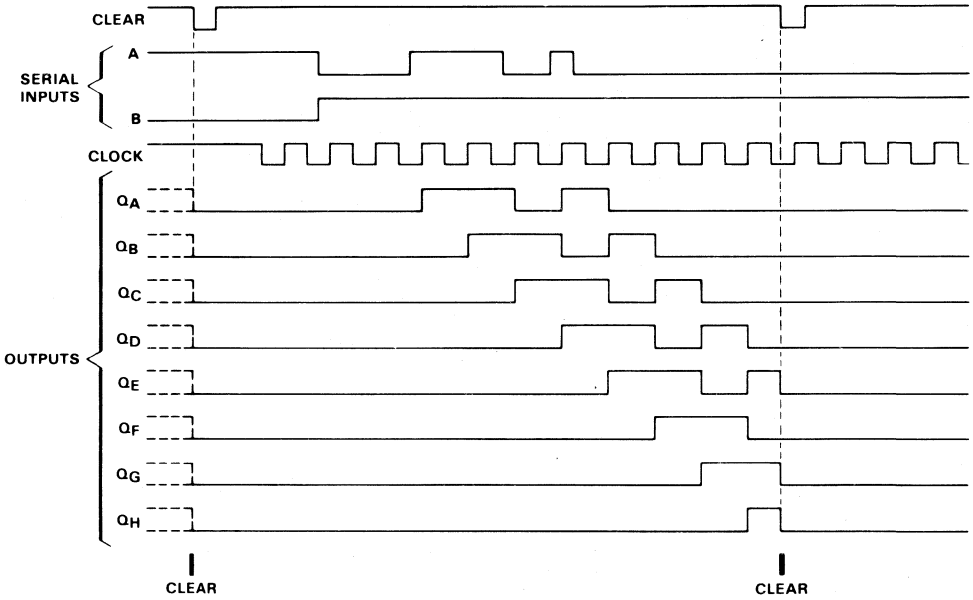
Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC164		74HC164		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PHL}	$\overline{CLR}$	ANY Q	2.0V 4.5V 6.0V			230 46 39		345 69 59		290 58 49	ns
t_{PLH}, t_{PHL}	CLK	ANY Q	2.0V 4.5V 6.0V			175 35 30		265 53 45		220 44 38	ns
t_r, t_f		Q	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
C_{pd}	Power dissipation capacitance per device at 25°C								140 typ		pF

4

typical clear, shift, and clear sequences



timing requirements (supplement to recommended operating conditions)

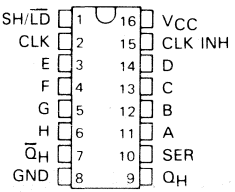
PARAMETER		CONDITIONS V_{CC}	54HC164			74HC164			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		3	0		4	MHz
		4.5V	0		16	0		20	
		6.0V	0		19	0		23	
t_w	$\overline{CLR}$ low	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	CLK high	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
	CLK low	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_{su}	Data	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	$\overline{CLR}$ inactive	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_h		2.0V	5			5			ns
		4.5V	5			5			
		6.0V	5			5			

TYPES SN54HC165, SN74HC165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

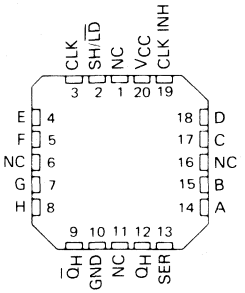
D2684, DECEMBER 1982

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC165 . . . J PACKAGE
SN74HC165 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC165 . . . FH OR FK PACKAGE
SN74HC165 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The 'HC165 also features a clock inhibit function and a complementary serial output Q_H.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

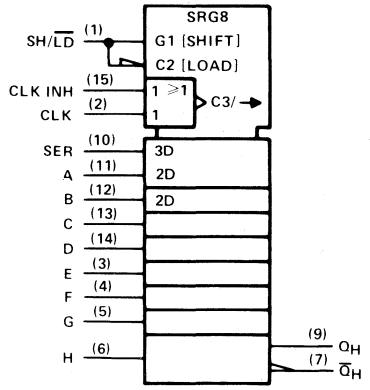
The SN54HC165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC165 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

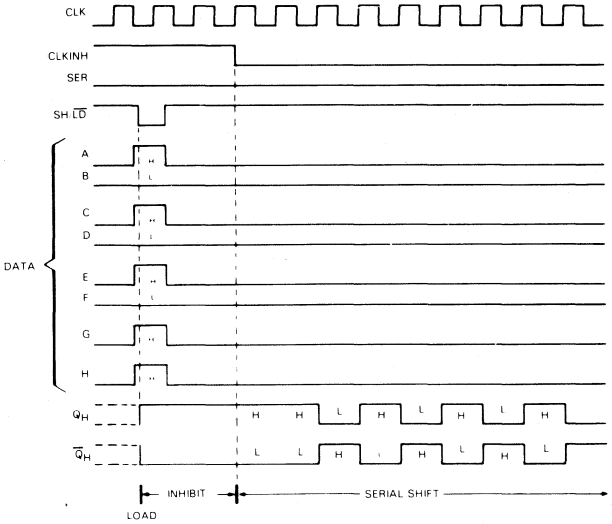
SHIFT – content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

logic symbol



Pin numbers shown are for J and N packages.

typical shift, load, and inhibit sequences



timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC165 MIN	54HC165 NOM	54HC165 MAX	74HC165 MIN	74HC165 NOM	74HC165 MAX	UNITS
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	SH/$\overline{LD}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	SH/$\overline{LD}$ high bef. CLK↑	2.0V 4.5V 6.0V	120 24 20			100 20 17			ns
	SER before CLK↑	2.0V 4.5V 6.0V	60 12 10			50 10 9			
	CLK INH bef. CLK↑	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	Data before SH/$\overline{LD}$↑	2.0V 4.5V 6.0V	60 12 10			50 10 9			
t_h	SER data after CLK↑	2.0V 4.5V 6.0V	0 0 0			0 0 0			ns
	Par. data after SH/$\overline{LD}$↑	2.0V 4.5V 6.0V	0 0 0			0 0 0			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC165		74HC165		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	SH/$\overline{LD}$	QH	2.0V 4.5V 6.0V			150 30 26		225 45 38		190 38 32	ns
t_{PLH}, t_{PHL}		$\overline{Q}$H	2.0V 4.5V 6.0V			150 30 26		225 45 38		190 38 32	ns
t_{PLH}, t_{PHL}	CLK	QH	2.0V 4.5V 6.0V			150 30 26		225 45 38		190 38 32	ns
t_{PLH}, t_{PHL}		$\overline{Q}$H	2.0V 4.5V 6.0V			150 30 26		225 45 38		190 38 32	ns
t_{PLH}, t_{PHL}	H	QH	2.0V 4.5V 6.0V			130 26 22		195 39 33		165 33 28	ns
t_{PLH}, t_{PHL}		$\overline{Q}$H	2.0V 4.5V 6.0V			130 26 22		195 39 33		165 33 28	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance at 25°C	29 typ	pF

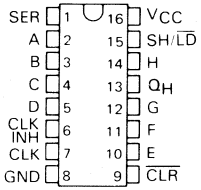
4

TYPES SN54HC166, SN74HC166
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

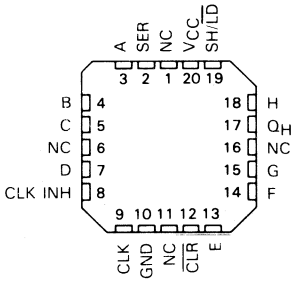
D2684, DECEMBER 1982

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC166 . . . J PACKAGE
SN74HC166 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC166 . . . FH OR FK PACKAGE
SN74HC166 . . . FH OR FN PACKAGE
(TOP VIEW)



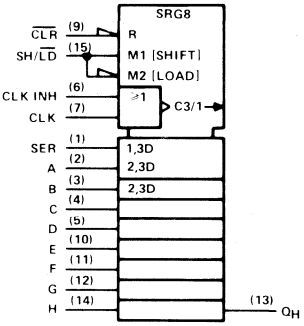
NC — No internal connection

description

The 'HC166 parallel-in or serial-in, serial-out registers feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN54HC166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC166 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

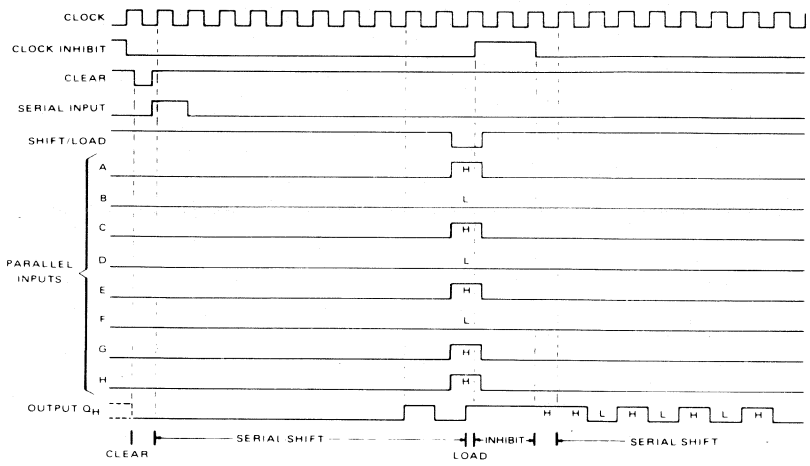
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

typical clear, shift, load, inhibit, and shift sequences



timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC166			74HC166			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V	0 0 0		3 16 19	0 0 0		4 20 23	MHz
t_w	$\overline{CLR}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	SH/$\overline{LD}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK high	2.0V 4.5V 6.0V	225 45 38			190 38 32			
	CLK low	2.0V 4.5V 6.0V	255 51 43			215 43 37			
t_{su}	SH/$\overline{LD}$ high	2.0V 4.5V 6.0V	190 38 32			155 31 26			ns
	SER	2.0V 4.5V 6.0V	205 41 35			170 34 29			
	CLK INH	2.0V 4.5V 6.0V	0 0 0			0 0 0			
	Data								
	$\overline{CLR}$ inactive	4.5V 6.0V	51 43			43 37			
t_h		2.0V 4.5V 6.0V	190 38 32			155 31 26			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC166		74HC166		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PHL}	$\overline{CLR}$	QH	2.0V 4.5V 6.0V			215 43 37		325 65 55		270 54 46	ns
t_{PD}	CLR	QH	2.0V 4.5V 6.0V			205 41 35		310 62 53		255 51 43	ns
t_{PD}	SH/$\overline{LD}$	QH	2.0V 4.5V 6.0V			195 39 33		295 59 50		245 49 42	ns
t_{PD}	H	QH	2.0V 4.5V 6.0V			210 42 36		315 63 54		265 53 45	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance at 25°C	60 typ	pF

4

TYPES SN54HC174, SN54HC175, SN74HC174, SN74HC175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

- **'HC174 Contains Six Flip-Flops with Single-Rail Outputs**
- **'HC175 Contains Four Flip-Flops with Double-Rail Outputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic, positive-edge-triggered D-type flip-flops have a direct clear input and the 'HC175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

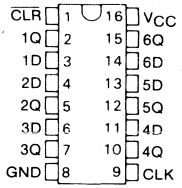
The SN54HC174 and SN54HC175 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC174 and SN74HC175 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

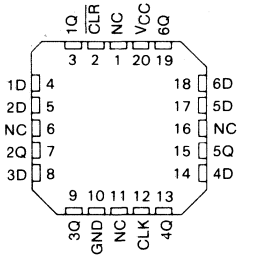
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

†'HC175 only

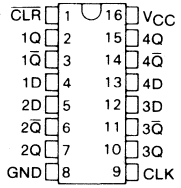
SN54HC174 . . . J PACKAGE
SN74HC174 . . . J OR N PACKAGE
(TOP VIEW)



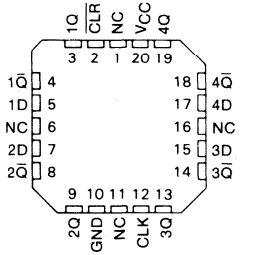
SN54HC174 . . . FH OR FK PACKAGE
SN74HC174 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC175 . . . J PACKAGE
SN74HC175 . . . J OR N PACKAGE
(TOP VIEW)



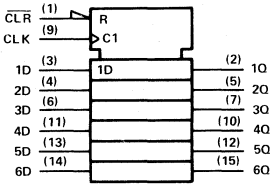
SN54HC175 . . . FH OR FK PACKAGE
SN74HC175 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

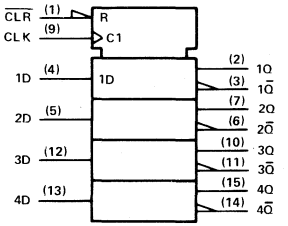
logic symbols

'HC174



Pin numbers shown are for J and N packages.

'HC175



timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC174 54HC175			74HC174 74HC175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	$\overline{CLR}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 30/25 for the 'HC175 21			
t_{su}	DATA	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	$\overline{CLR}$ Inactive	2.0V 4.5V 6.0V	60 12 10			50 10 9			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC174		74HC174		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	$\overline{CLR}$	Q	2.0V 4.5V 6.0V			160 32 27		240 48 41		200 40 34	ns
t_{PLH}, t_{PHL}	CLK	Q	2.0V 4.5V 6.0V			160 32 27		240 48 41		200 40 34	ns
t_r, t_f		Q	2.0V 4.5V 6.0V			75 15 13		110 22 19		90 19 16	ns

C_{pd}	Power dissipation capacitance per flip-flop at 25°C	27 typ	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC175		74HC175		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V	5			3		4		MHz
			4.5V	25			16		20		
			6.0V	29			19		23		
t_{PLH}, t_{PHL}	$\overline{CLR}$	Q, $\overline{Q}$	2.0V	170			255		215		ns
			4.5V	34			51		43		
			6.0V	29			43		37		
t_{PLH}, t_{PHL}	CLK	Q, $\overline{Q}$	2.0V	150			255		190		ns
			4.5V	30			45		38		
			6.0V	26			38		32		
t_r, t_f		Q, $\overline{Q}$	2.0V			75		110		90	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

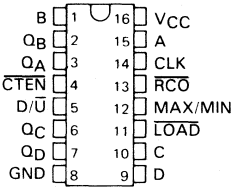
C_{pd}	Power dissipation capacitance per flip-flop at 25°C	30 typ	pF

TYPES SN54HC190, SN54HC191, SN74HC190, SN74HC191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

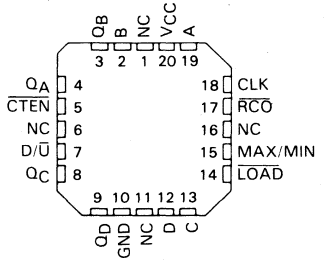
D2684, DECEMBER 1982

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC190, SN54HC191 . . . J PACKAGE
SN74HC190, SN74HC191 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC190, SN54HC191 . . . FH OR FK PACKAGE
SN74HC190, SN74HC191 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC190 and 'HC191 are synchronous, reversible up/down counters. The 'HC190 is a 4-bit decade counter and the 'HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

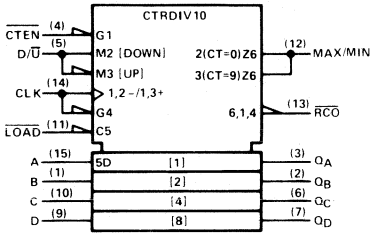
These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54HC190 and SN54HC191 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC190 and SN74HC191 are characterized for operation from −40°C to 85°C.

'HC190 logic symbol

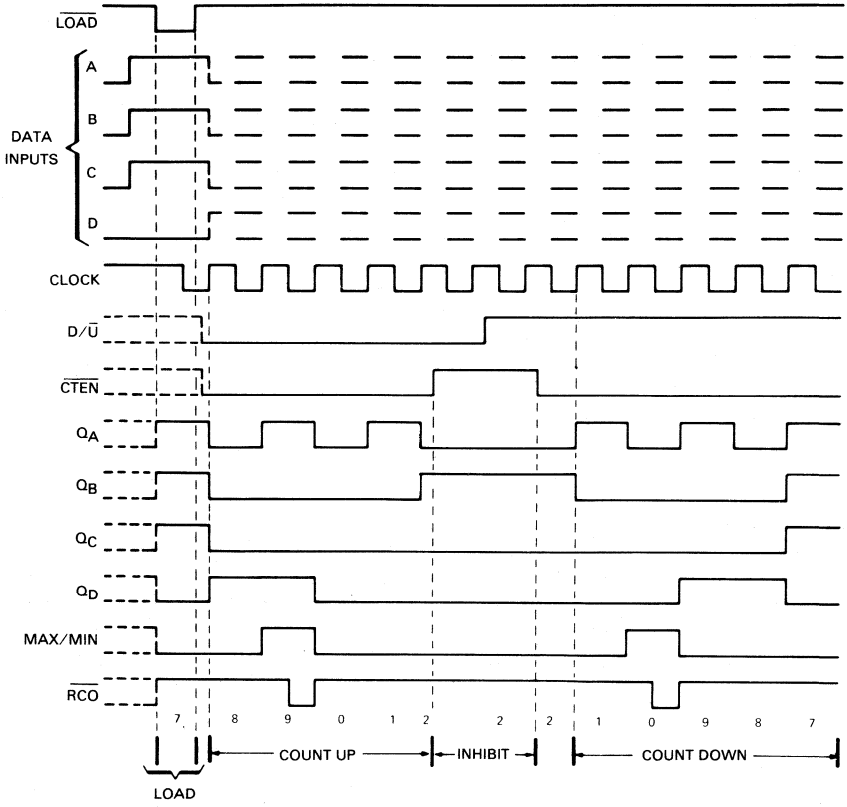


Pin numbers shown are for J and N packages.

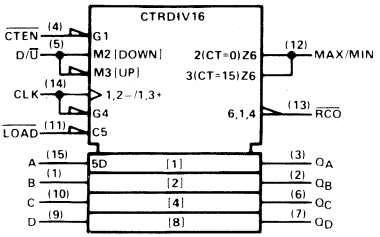
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



'HC191 logic symbol

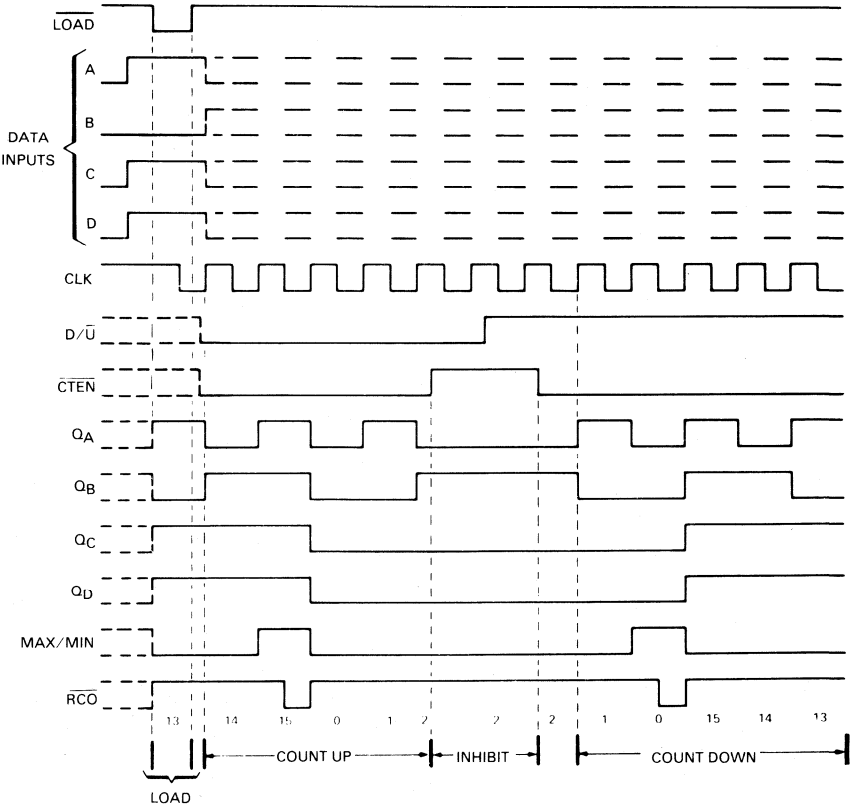


Pin numbers shown are for J and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC190 54HC191		74HC190 74HC191		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	4 21 24			2.5 13 16		3 16 19		MHz
t_{PLH}, t_{PHL}	$\overline{LOAD}$	ANY Q	2.0V 4.5V 6.0V			264 53 45		396 79 67		330 66 56	ns
t_{PLH}, t_{PHL}	A,B, C,D	ANY Q	2.0V 4.5V 6.0V			240 48 41		360 72 61		300 60 51	ns
t_{PLH}, t_{PHL}	CLK	$\overline{RCO}$	2.0V 4.5V 6.0V			120 24 21		180 36 31		150 30 26	ns
t_{PLH}, t_{PHL}	CLK	ANY Q	2.0V 4.5V 6.0V			192 38 32		288 58 49		240 48 41	ns
t_{PLH}, t_{PHL}	CLK	MAX/ MIN	2.0V 4.5V 6.0V			252 50 43		378 76 65		315 63 54	ns
t_{PLH}, t_{PHL}	D/$\overline{U}$	$\overline{RCO}$	2.0V 4.5V 6.0V			228 46 38		342 68 59		285 57 49	ns
t_{PLH}, t_{PHL}	D/$\overline{U}$	MAX/ MIN	2.0V 4.5V 6.0V			192 38 32		288 58 49		240 48 41	ns
t_{PLH}, t_{PHL}	$\overline{CTEN}$	$\overline{RCO}$	2.0V 4.5V 6.0V			132 26 23		198 40 34		165 33 28	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			90 18 16		132 26 23		110 22 19	ns
C_{pd}	Power dissipation capacitance at 25°C								70 typ		pF

timing requirements (supplement to recommended operating conditions)

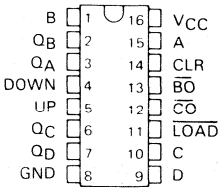
PARAMETER		CONDITIONS V_{CC}	54HC190 54HC191			74HC190 74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V	0 0 0		2.5 13 16	0 0 0		3 16 19	MHz
t_w	$\overline{LOAD}$ low	2.0V 4.5V 6.0V	180 36 31			150 30 26			ns
	CLK high	2.0V 4.5V 6.0V	180 36 31			150 30 26			
	CLK low	2.0V 4.5V 6.0V	180 36 31			150 30 26			
t_{su}	Data before $\overline{LOAD}$	2.0V 4.5V 6.0V	256 46 38			188 38 32			ns
	$\overline{CTEN}$ before CLK	2.0V 4.5V 6.0V	306 61 53			255 51 44			
	D/$\overline{U}$ before CLK	2.0V 4.5V 6.0V	306 61 53			255 51 44			
	$\overline{LOAD}$ inactive	2.0V 4.5V 6.0V	256 46 38			188 38 32			
t_h	Data after $\overline{LOAD}$	2.0 4.5V 6.0V	5 5 5			5 5 5			ns
	$\overline{CTEN}$ after CLK	2.0V 4.5V 6.0V	5 5 5			5 5 5			
	D/$\overline{U}$ after CLK	2.0V 4.5V 6.0V	5 5 5			5 5 5			

TYPES SN54HC192, SN54HC193, SN74HC192, SN74HC193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

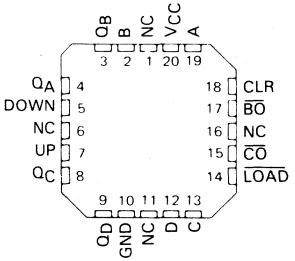
D2684, DECEMBER 1982

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC192, SN54HC193 . . . J PACKAGE
SN74HC192, SN74HC193 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC192, SN54HC193 . . . FH OR FK PACKAGE
SN74HC192, SN74HC193 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC192 and 'HC193 are synchronous, reversible up/down counters. The 'HC192 is a 4-bit decade counter and the 'HC193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

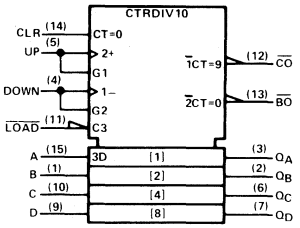
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54HC192 and SN54HC193 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC192 and SN74HC193 are characterized for operation from -40°C to 85°C.

'HC192 logic symbol

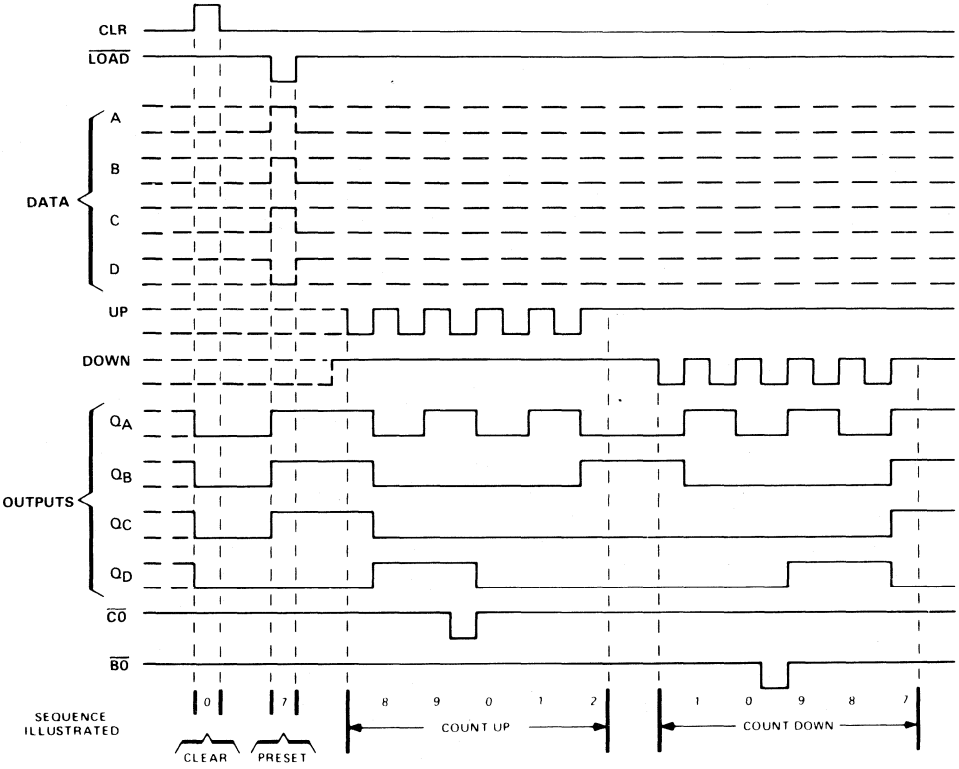


Pin numbers shown are for J and N packages.

typical clear, load, and count sequences

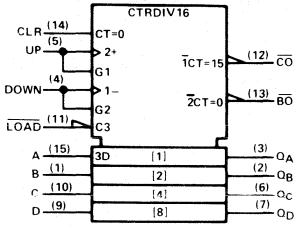
Illustrated below is the following:

1. Clear outputs to zero.
2. Load (preset) BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'HC193 logic symbol

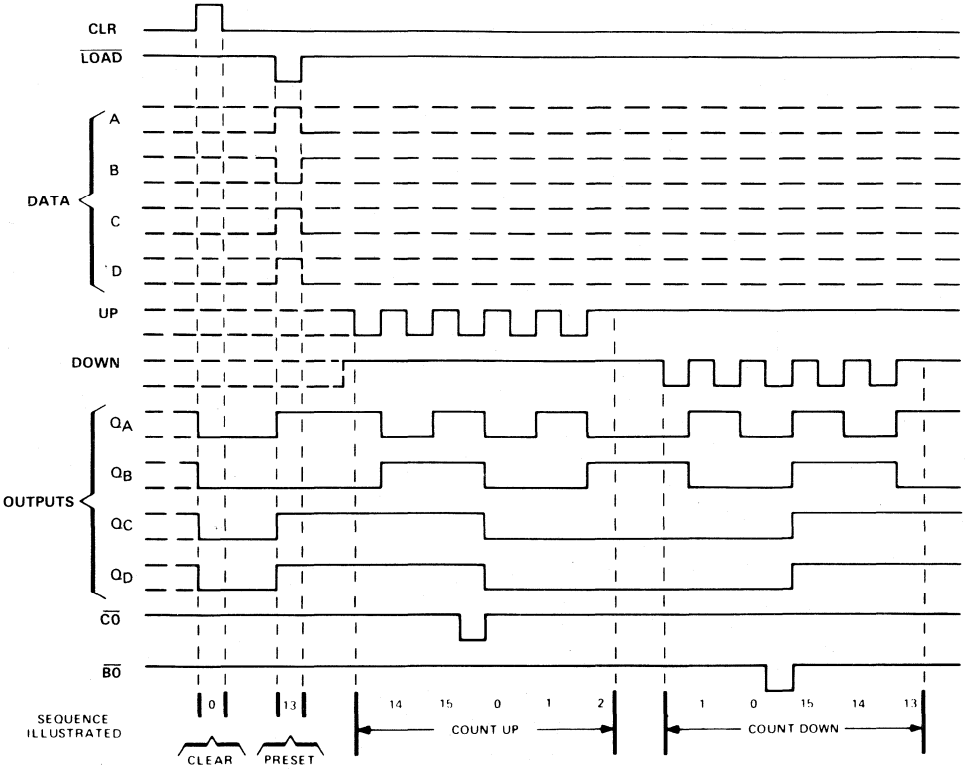


Pin numbers shown are for J and N packages.

typical clear, load, and count sequences

Illustrated below is the following:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC192 54HC193			74HC192 74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		2.5	0		3	MHz
		4.5V	0		13	0		16	
		6.0V	0		16	0		19	
t_w	CLR high	2.0V	180			150			ns
		4.5V	36			30			
		6.0V	31			26			
	$\overline{LOAD}$ low	2.0V	180			150			
		4.5V	36			30			
		6.0V	31			26			
	UP or DOWN high	2.0V	180			150			
		4.5V	36			30			
		6.0V	31			26			
	UP or DOWN low	2.0V	180			150			
		4.5V	36			30			
		6.0V	31			26			
t_{su}	Data before $\overline{LOAD}$	2.0V	226			188			ns
		4.5V	46			38			
		6.0V	38			32			
	CLR inactive	2.0V	226			188			
		4.5V	46			38			
		6.0V	38			32			
	$\overline{LOAD}$ inactive	2.0V	226			188			
		4.5V	46			38			
		6.0V	38			32			
t_h	Data after $\overline{LOAD}$	2.0	5			5			ns
		4.5V	5			5			
		6.0V	5			5			
	UP high after DOWN	2.0V	5			5			
		4.5V	5			5			
		6.0V	5			5			
	DOWN high after UP	2.0V	5			5			
		4.5V	5			5			
		6.0V	5			5			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC192 54HC193		74HC192 74HC193		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V	4			2.5		3		MHz
			4.5V	21			13		16		
			6.0V	24			16		19		
t_{PLH}, t_{PHL}	UP	$\overline{CO}$	2.0V			132		198		165	ns
			4.5V			26		40		33	
			6.0V			23		34		28	
t_{PLH}, t_{PHL}	DOWN	$\overline{BO}$	2.0V			132		198		165	ns
			4.5V			26		40		33	
			6.0V			23		34		28	
t_{PLH}, t_{PHL}	UP or DOWN	ANY Q	2.0V			204		306		255	ns
			4.5V			41		61		51	
			6.0V			35		52		43	
t_{PLH}, t_{PHL}	$\overline{LOAD}$	ANY Q	2.0V			180		270		225	ns
			4.5V			36		54		45	
			6.0V			31		46		38	
t_{PLH}, t_{PHL}	CLR	ANY Q	2.0V			180		270		225	ns
			4.5V			36		54		45	
			6.0V			31		46		38	
t_r, t_f		ANY	2.0V			90		132		110	ns
			4.5V			18		26		22	
			6.0V			16		23		19	

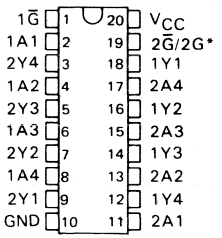
C_{pd}	Power dissipation capacitance at 25°C	70 typ	pF

TYPES SN54HC240, SN54HC241, SN74HC240, SN74HC241, SN54HCT240*, SN54HCT241,* SN74HCT240*, SN74HCT241* OCTAL BUFFERS AND LINE DRIVFRS WITH 3-STATE OUTPUTS

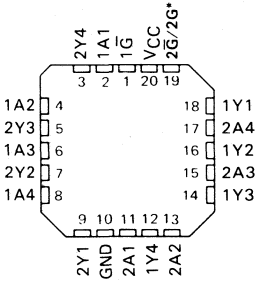
D2684, DECEMBER 1982

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC' . . . J PACKAGE
SN74HC' . . . J OR N PACKAGE
(TOP VIEW)



SN54HC' . . . FH OR FK PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



*2G̅ for 'HC240, or 2G for 'HC241

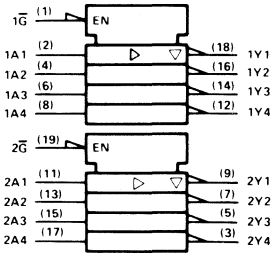
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G̅ (active-low output control) inputs, and complementary G and G̅ inputs. These devices feature high fan-out.

The SN54HC' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC' family is characterized for operation from -40°C to 85°C.

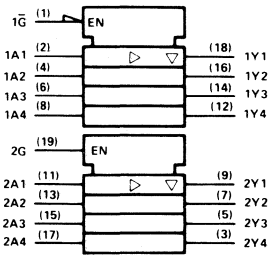
logic symbols

'HC240



Pin numbers shown are for J and N packages.

'HC241



*) PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC240 54HCT240		74HC240 74HCT240		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	50 pF	2.0V			125		185		160	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			25		37		32	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			21		31		27	
			150 pF	6.0V			36		53		46	
t_{PHL}			50 pF	2.0V			125		185		160	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			25		37		32	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			21		31		27	
			150 pF	6.0V			36		53		46	
t_{PZH}	$\overline{G}$	Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PZL}			50 pF	2.0V			175		265		220	
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PLZ}	$\overline{G}$	Y	50 pF	2.0V			175		265		220	ns
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_{PHZ}			50 pF	2.0V			175		265		220	
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per buffer at 25°C	typ	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC241 54HCT241		74HC241 74HCT241		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	50 pF	2.0V			125		185		160	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			25		37		32	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			21		31		27	
			150 pF	6.0V			36		53		46	
t_{PHL}			50 pF	2.0V			125		185		160	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			25		37		32	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			21		31		27	
			150 pF	6.0V			36		53		46	
t_{PZH}	$1\overline{G}$	1Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PZL}			50 pF	2.0V			175		265		220	
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PLZ}	$1\overline{G}$	1Y	50 pF	2.0V			175		265		220	ns
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_{PHZ}			50 pF	2.0V			175		265		220	
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_{PZH}	$2\overline{G}$	2Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PZL}			50 pF	2.0V			175		265		220	
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PLZ}	$2\overline{G}$	2Y	50 pF	2.0V			175		265		220	ns
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_{PHZ}			50 pF	2.0V			175		265		220	
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_r		1Y or 2Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

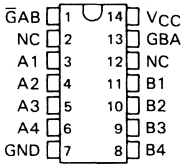
C_{pd}	Power dissipation capacitance per buffer at 25°C	typ	pF

TYPES SN54HC242, SN54HC243, SN74HC242, SN74HC243, SN54HCT242*, SN54HCT243*, SN74HCT242*, SN74HCT243* QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

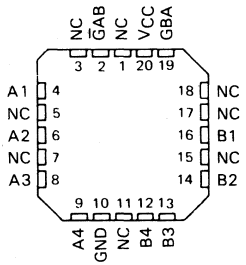
D2684, DECEMBER 1982

- **2-Way Asynchronous Communication Between Data Buses**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC242, SN54HC243 . . . J PACKAGE
SN74HC242, SN74HC243 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC242, SN54HC243 . . . FH OR FK PACKAGE
SN74HC242, SN74HC243 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74HC' devices can be used to drive terminated lines down to 133 ohms.

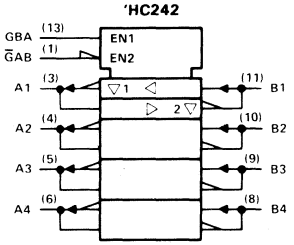
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from -40°C to 85°C.

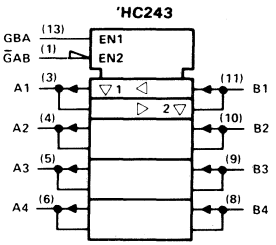
The '242 is the inverting version of the '243.

FUNCTION TABLE

INPUTS		'HC242	'HC243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

logic symbol





Pin numbers shown are for J and N packages.

*) PRODUCT PREVIEW

'HC242 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC242 54HCT242		74HC242 74HCT242		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PHL}			50 pF	2.0V			150		225		190	
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PZH}	$\overline{G}AB$	B	50 pF	2.0V			200		300		250	ns
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PZL}			50 pF	2.0V			200		300		250	
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PLZ}	$\overline{G}AB$	B	50 pF	2.0V			200		300		250	ns
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PHZ}			50 pF	2.0V			200		300		250	
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PZH}	GBA	A	50 pF	2.0V			200		300		250	ns
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PZL}			50 pF	2.0V			200		300		250	
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PLZ}	GBA	A	50 pF	2.0V			200		300		250	ns
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PHZ}			50 pF	2.0V			200		300		250	
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per TXCVR at 25°C	34 typ	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC243 54HCT243		74HC243 74HCT243		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PHL}			50 pF	2.0V			150		225		190	
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PZH}	$\overline{G}AB$	B	50 pF	2.0V			200		300		250	ns
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PZL}			50 pF	2.0V			200		300		250	
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PLZ}	$\overline{G}AB$	B	50 pF	2.0V			200		300		250	ns
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PHZ}			50 pF	2.0V			200		300		250	
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PZH}	GBA	A	50 pF	2.0V			200		300		250	ns
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PZL}			50 pF	2.0V			200		300		250	
			150 pF	2.0V			285		430		355	
			50 pF	4.5V			40		60		50	
			150 pF	4.5V			57		86		71	
			50 pF	6.0V			34		51		43	
			150 pF	6.0V			49		73		62	
t_{PLZ}	GBA	A	50 pF	2.0V			200		300		250	ns
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_{PHZ}			50 pF	2.0V			200		300		250	
			50 pF	4.5V			40		60		50	
			50 pF	6.0V			34		51		43	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per TXCVR at 25°C	34 typ	pF

TYPES SN54HC244, SN74HC244, SN54HCT244*, SN74HCT244* OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

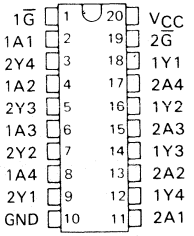
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

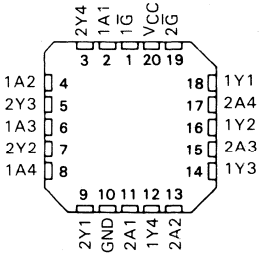
These octal buffers and line drivers are designed specifically to improve both the performance and density of the three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'HC240 and 'HC241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

The SN54HC244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC244 is characterized for operation from -40°C to 85°C.

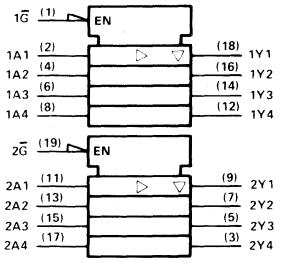
SN54HC244 . . . J PACKAGE
SN74HC244 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC244 . . . FH OR FK PACKAGE
SN74HC244 . . . FH OR FN PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown are for J and N packages.

*) PRODUCT PREVIEW

HC244 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC244 54HCT244		74HC244 74HCT244		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	50 pF	2.0V			140		210		175	ns
			150 pF	2.0V			230		340		280	
			50 pF	4.5V			28		42		35	
			150 pF	4.5V			45		68		56	
			50 pF	6.0V			24		36		30	
			150 pF	6.0V			39		58		49	
t_{PHL}			50 pF	2.0V			140		210		175	
			150 pF	2.0V			230		340		280	
			50 pF	4.5V			28		42		35	
			150 pF	4.5V			45		68		56	
			50 pF	6.0V			24		36		30	
			150 pF	6.0V			39		58		49	
t_{PZH}	$\overline{G}$	Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PZL}			50 pF	2.0V			175		265		220	
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		65	
			50 pF	6.0V			30		45		38	
			150 pF	6.0V			45		67		57	
t_{PLZ}	$\overline{G}$	Y	50 pF	2.0V			175		265		220	ns
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_{PHZ}			50 pF	2.0V			175		265		220	
			50 pF	4.5V			35		53		44	
			50 pF	6.0V			30		45		38	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

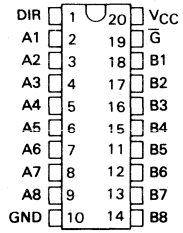
C_{pd}	Power dissipation capacitance per buffer at 25°C	34 typ	pF

TYPES SN54HC245, SN74HC245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

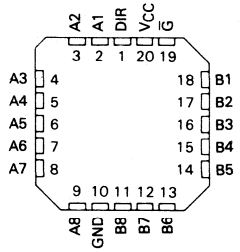
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC245 . . . J PACKAGE
SN74HC245 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC245 . . . FH OR FK PACKAGE
SN74HC245 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

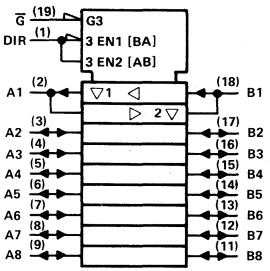
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54HC245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC245		74HC245		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			140		210		175	ns
			150 pF	2.0V			225		340		280	
			50 pF	4.5V			28		42		35	
			150 pF	4.5V			45		68		56	
			50 pF	6.0V			24		36		30	
			150 pF	6.0V			39		58		49	
t_{PHL}			50 pF	2.0V			140		210		175	
			150 pF	2.0V			225		340		280	
			50 pF	4.5V			28		42		35	
			150 pF	4.5V			45		68		56	
			50 pF	6.0V			24		36		30	
			150 pF	6.0V			39		58		49	
t_{PZH}	$\overline{G}$	A or B	50 pF	2.0V			230		340		290	ns
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PZL}			50 pF	2.0V			230		340		290	
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PLZ}	$\overline{G}$	A or B	50 pF	2.0V			230		340		290	ns
			50 pF	4.5V			46		68		58	
			50 pF	6.0V			39		58		49	
t_{PHZ}			50 pF	2.0V			230		340		290	
			50 pF	4.5V			46		68		58	
			50 pF	6.0V			39		58		49	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

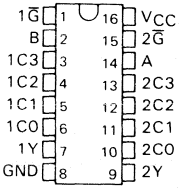
C_{pd}	Power dissipation capacitance per TXCVR at 25°C	typ	pF

TYPES SN54HC253, SN74HC253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

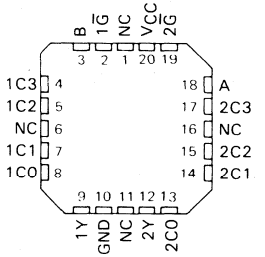
D2684, DECEMBER 1982

- **3-State Versions of 'HC153**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC253 . . . J PACKAGE
SN74HC253 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC253 . . . FH OR FK PACKAGE
SN74HC253 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

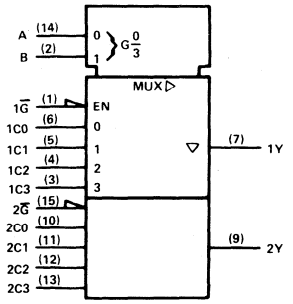
The SN54HC253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC253 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC253		74HC253		UNIT
			CL	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A or B	Y	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PLH}, t_{PHL}	DATA (ANY C)	Y	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PZH}, t_{PZL}	$\overline{G}$	Y	50 pF	2.0V			100		150		125	ns
			150 pF	2.0V			185		280		230	
			50 pF	4.5V			20		30		25	
			150 pF	4.5V			37		56		46	
			50 pF	6.0V			17		26		21	
			150 pF	6.0V			32		48		40	
t_{PLZ}, t_{PHZ}	$\overline{G}$	Y	50 pF	2.0V			100		150		125	ns
			50 pF	4.5V			20		30		25	
			50 pF	6.0V			17		26		21	
t_r, t_f		ANY	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

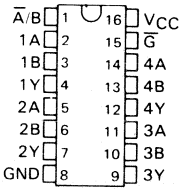
C_{pd}	Power dissipation capacitance per MUX. at 25°C	typ	pF

TYPES SN54HC257, SN54HC258, SN74HC257, SN74HC258 QUAD 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive up to 15 LSTTL Loads**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC257, SN54HC258 . . . J PACKAGE
SN74HC257, SN74HC258 . . . J OR N PACKAGE
(TOP VIEW)

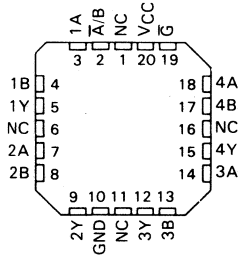


description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level..

The SN54HC257 and SN54HC258 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC257 and SN74HC258 are characterized for operation from −40°C to 85°C.

SN54HC257, SN54HC258 . . . FH OR FK PACKAGE
SN74HC257, SN74HC258 . . . FH OR FN PACKAGE
(TOP VIEW)



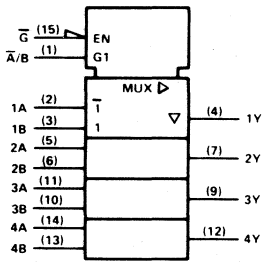
NC — No internal connection

FUNCTION TABLE

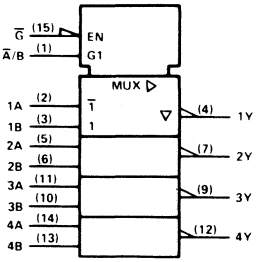
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	'HC257	'HC258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic symbols

'HC257



'HC258



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

'HC257 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC257		74HC257		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PD}	A or B	ANY Y	50 pF	2.0V			95		145		120	ns
			150 pF	2.0V			180		275		225	
			50 pF	4.5V			19		29		24	
			150 pF	4.5V			36		55		45	
			50 pF	6.0V			16		25		20	
			150 pF	6.0V			31		47		39	
t_{PD}	$\overline{A}$/B	ANY Y	50 pF	2.0V			115		175		145	ns
			150 pF	2.0V			200		305		250	
			50 pF	4.5V			23		35		29	
			150 pF	4.5V			40		61		50	
			50 pF	6.0V			20		30		25	
			150 pF	6.0V			35		52		44	
t_{PZH}, t_{PZL}	$\overline{G}$	ANY Y	50 pF	2.0V			160		240		200	ns
			150 pF	2.0V			245		370		305	
			50 pF	4.5V			32		48		40	
			150 pF	4.5V			49		74		61	
			50 pF	6.0V			27		41		34	
			150 pF	6.0V			42		63		53	
t_{PLZ}, t_{PHZ}	$\overline{G}$	ANY Y	50 pF	2.0V			160		240		200	ns
			50 pF	4.5V			32		48		40	
			50 pF	6.0V			27		41		34	
t_t		ANY	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per MUX at 25°C	typ	pF

'HC258 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC258		74HC258		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PD}	A or B	ANY Y	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PD}	$\overline{A}$/B	ANY Y	50 pF	2.0V			115		175		145	ns
			150 pF	2.0V			200		305		250	
			50 pF	4.5V			23		35		29	
			150 pF	4.5V			40		61		50	
			50 pF	6.0V			20		30		25	
			150 pF	6.0V			35		52		44	
t_{PZH}, t_{PZL}	$\overline{G}$	ANY Y	50 pF	2.0V			150		225		190	ns
			150 pF	2.0V			235		355		295	
			50 pF	4.5V			30		45		38	
			150 pF	4.5V			47		71		59	
			50 pF	6.0V			26		38		32	
			150 pF	6.0V			41		60		51	
t_{PLZ}, t_{PHZ}	$\overline{G}$	ANY Y	50 pF	2.0V			150		225		190	ns
			50 pF	4.5V			30		45		38	
			50 pF	6.0V			26		38		32	
t_t		ANY	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per MUX at 25°C	typ	pF

TYPES SN54HC266, SN74HC266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

D2684, DECEMBER 1982

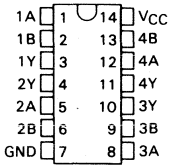
- **Can Be Used as a 4-Bit Digital Comparator**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

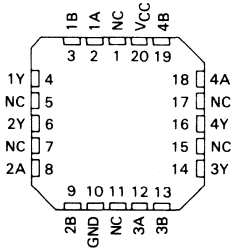
The 'HC266 is composed of four independent 2-input exclusive-NOR gates. While pin-compatible with the 'LS266, the 'HC266 has totem-pole outputs rather than open-collector.

The SN54HC266 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC266 is characterized for operation from −40°C to 85°C.

SN54HC266 . . . J PACKAGE
SN74HC266 . . . J OR N PACKAGE
(TOP VIEW)

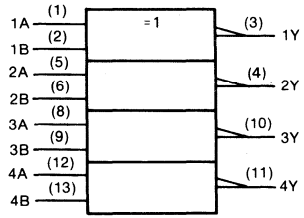


SN54HC266 . . . FH OR FK PACKAGE
SN74HC266 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC266		74HC266		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

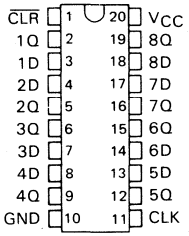
C_{pd}	Power dissipation capacitance per gate at 25°C	40 typ	pF

TYPES SN54HC273, SN74HC273
OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

- **Contains Eight Flip-Flops with Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC273 . . . J PACKAGE
SN74HC273 . . . J OR N PACKAGE
(TOP VIEW)



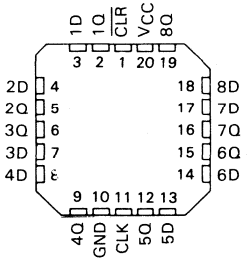
description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54HC273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC273 is characterized for operation from −40°C to 85°C.

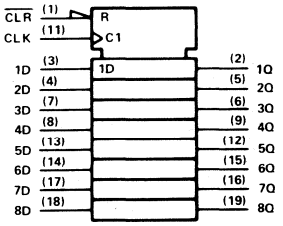
SN54HC273 . . . FH OR FK PACKAGE
SN74HC273 . . . FH OR FN PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol



Pin numbers shown are for all packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC273			74HC273			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	$\overline{CLR}$ low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
	CLK high	2.0V 4.5V 6.0V	150 30 25			125 25 21			
	CLK low	2.0V 4.5V 6.0V	150 30 25			125 25 21			
t_{su}	Data	2.0V 4.5V 6.0V	165 33 28			140 28 24			ns
	$\overline{CLR}$ inactive	2.0V 4.5V 6.0V	150 30 31			125 25 27			
t_h		2.0V 4.5V 6.0V	5 5 5			5 5 5			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC273		74HC273		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PHL}	$\overline{CLR}$	ANY	2.0V 4.5V 6.0V			165 33 28		250 50 43		205 41 35	ns
t_{PLH}, t_{PHL}	CLK	ANY	2.0V 4.5V 6.0V			175 35 30		265 53 45		220 44 37	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	28 typ	pF

TYPES SN54HC280, SN74HC280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

D2684, DECEMBER 1982

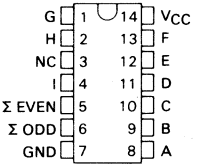
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits**
- **Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

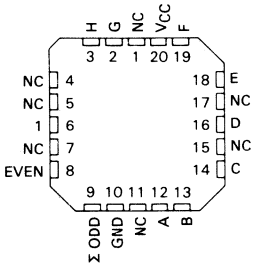
These universal, monolithic, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The SN54HC280 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC280 is characterized for operation from −40°C to 85°C.

SN54HC280 . . . J PACKAGE
SN74HC280 . . . J OR N PACKAGE
(TOP VIEW)

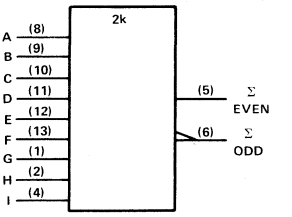


SN54HC280 . . . FH OR FK PACKAGE
SN74HC280 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

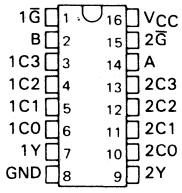
PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC280		74HC280		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PD}	Data	Sigma even	2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		ns
t_{PD}	Data	Sigma odd	2.0V 4.5V 6.0V			175 35 30		265 53 45		220 44 37	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns
C_{pd}	Power dissipation capacitance at 25°C								33 typ		pf

TYPES SN54HC352, SN74HC352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

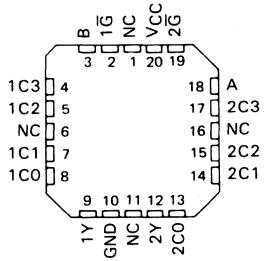
D2684, DECEMBER 1982

- **Inverting Versions of 'HC153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC352 . . . J PACKAGE
SN74HC352 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC352 . . . FH OR FK PACKAGE
SN74HC352 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The SN54HC352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC352 is characterized for operation from −40°C to 85°C.

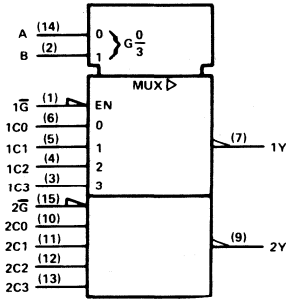
4

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC352		74HC352		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	50 pF	2.0V			185		280		230	ns
			150 pF	2.0V			270		410		335	
			50 pF	4.5V			37		56		46	
			150 pF	4.5V			54		82		67	
			50 pF	6.0V			32		48		39	
			150 pF	6.0V			47		70		58	
t_{PHL}			50 pF	2.0V			185		280		230	
			150 pF	2.0V			270		410		335	
			50 pF	4.5V			37		56		46	
			150 pF	4.5V			54		82		67	
			50 pF	6.0V			32		48		39	
			150 pF	6.0V			47		70		58	
t_{PLH}	DATA (ANY C)	Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		63	
			50 pF	6.0V			30		45		37	
			150 pF	6.0V			45		67		56	
t_{PHL}			50 pF	2.0V			175		265		220	
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		63	
			50 pF	6.0V			30		45		37	
			150 pF	6.0V			45		67		56	
t_{PLH}, t_{PHL}	$\overline{G}$	Y	50 pF	2.0V			135		205		170	ns
			150 pF	2.0V			220		335		275	
			50 pF	4.5V			27		41		34	
			150 pF	4.5V			44		67		55	
			50 pF	6.0V			23		35		29	
			150 pF	6.0V			38		57		48	
t_r		Y	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

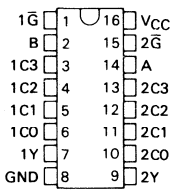
C_{pd}	Power dissipation capacitance per MUX. at 25°C	typ	pF

TYPES SN54HC353, SN74HC353
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

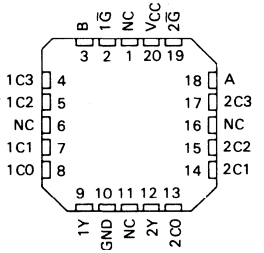
D2684, DECEMBER 1982

- **Inverting Versions of 'HC253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC353 . . . J PACKAGE
SN74HC353 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC353 . . . FH OR FK PACKAGE
SN74HC353 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enable output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

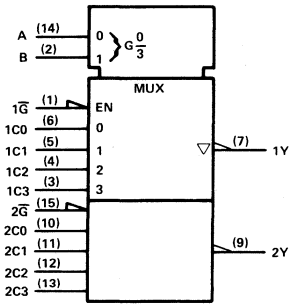
The SN54HC353 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC353 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC353		74HC353		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A or B	Y	50 pF	2.0V			185		280		230	ns
			150 pF	2.0V			270		410		335	
			50 pF	4.5V			37		56		46	
			150 pF	4.5V			54		82		67	
			50 pF	6.0V			32		48		39	
			150 pF	6.0V			47		70		58	
t_{PLH}, t_{PHL}	DATA (ANY C)	Y	50 pF	2.0V			175		265		220	ns
			150 pF	2.0V			260		395		325	
			50 pF	4.5V			35		53		44	
			150 pF	4.5V			52		79		63	
			50 pF	6.0V			30		45		37	
			150 pF	6.0V			45		67		56	
t_{PZH}, t_{PZL}	$\overline{G}$	Y	50 pF	2.0V			135		205		170	ns
			150 pF	2.0V			220		335		275	
			50 pF	4.5V			27		41		34	
			150 pF	4.5V			44		67		55	
			50 pF	6.0V			23		35		29	
			150 pF	6.0V			38		57		48	
t_{PLZ}, t_{PHZ}	$\overline{G}$	Y	50 pF	2.0V			135		205		170	ns
			50 pF	4.5V			27		41		34	
			50 pF	6.0V			23		35		29	
t_r, t_f		ANY	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per MUX, at 25°C	90 typ	pF

4

HIGH-SPEED CMOS LOGIC

TYPES SN54HC365 THRU SN54HC368, SN74HC365 THRU SN54HC368 HEX BUS DRIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or up to 15 LSTTL Loads**
- **Choice of True or Inverting Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

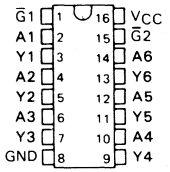
'HC365, 'HC367	True Outputs
'HC366, 'HC368	Inverting Outputs

description

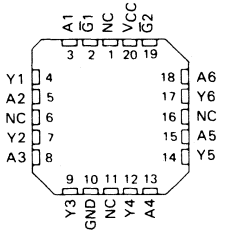
These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G (active-low control) inputs.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from −40°C to 85°C.

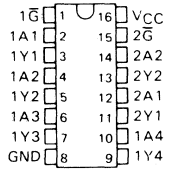
SN54HC365, SN54HC366 . . . J PACKAGE
SN74HC365, SN74HC366 . . . J OR N PACKAGE
(TOP VIEW)



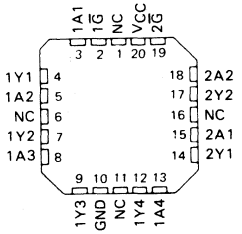
SN54HC367, SN54HC368 . . . FH OR FK PACKAGE
SN74HC367, SN74HC368 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC367, SN54HC368 . . . J PACKAGE
SN74HC367, SN74HC368 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC365, SN54HC366 . . . FH OR FK PACKAGE
SN74HC368, SN74HC366 . . . FH OR FN PACKAGE
(TOP VIEW)

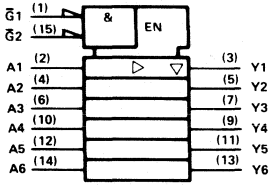


NC — No internal connection

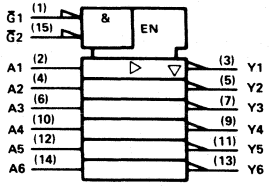
TEXAS INSTRUMENTS

logic symbols

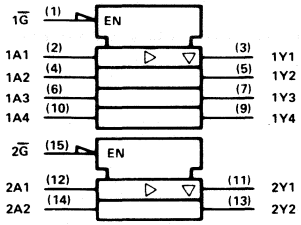
'HC365



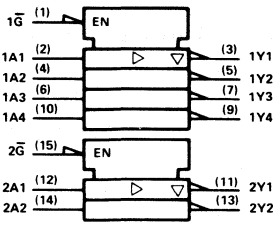
'HC366



'HC367



'HC368



Pin numbers shown are for J and N packages.

'HC366, 'HC368 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC365 thru 54HC368		74HC365 thru 74HC368		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	Y	50pF	2.0V			110		165		140	ns
			150pF	2.0V			195		295		245	
			50pF	4.5V			22		33		28	
			150pF	4.5V			39		59		49	
			50pF	6.0V			19		28		24	
			150pF	6.0V			34		50		43	
t_{PZH}, t_{PZL}	$\overline{G}$	Y	50pF	2.0V			220		330		280	ns
			150pF	2.0V			305		460		385	
			50pF	4.5V			44		66		56	
			150pF	4.5V			61		92		77	
			50pF	6.0V			38		56		48	
			150pF	6.0V			53		78		67	
t_{PHZ}, t_{PLZ}	$\overline{G}$	Y	50pF	2.0V			220		330		280	ns
			50pF	4.5V			44		66		56	
			50pF	6.0V			38		56		48	
t_r, t_f		ANY	50pF	2.0V			60		90		75	ns
			150pF	2.0V			210		315		265	
			50pF	4.5V			12		18		15	
			150pF	4.5V			42		63		53	
			50pF	6.0V			10		15		13	
			150pF	6.0V			36		53		45	

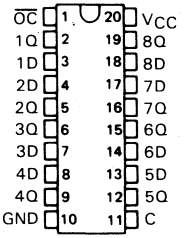
C_{pd}	Power dissipation capacitance per driver at 22°C	22 typ	pF

TYPES SN54HC373, SN74HC373
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

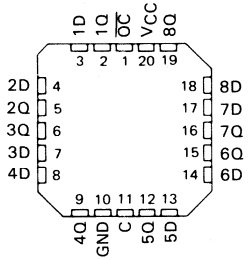
D2684, DECEMBER 1982

- **8 High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC373 . . . J PACKAGE
SN74HC373 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC373 . . . FH OR FK PACKAGE
SN74HC373 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

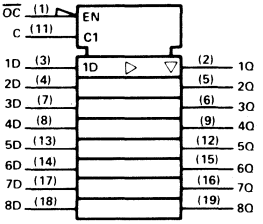
The eight latches of the 'HC373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC373 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC373			74HC373			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	2.0V	150			125			ns
	4.5V	30			25			
	6.0V	25			21			
t_{su}	2.0V	75			63			ns
	4.5V	15			13			
	6.0V	13			11			
t_h	2.0V	5			5			ns
	4.5V	5			5			
	6.0V	5			5			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

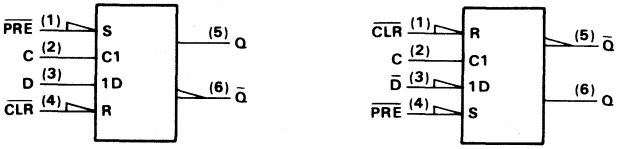
PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC373		74HC373		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	D	Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PLH}, t_{PHL}	C	ANY Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PZH}, t_{PZL}	OC	ANY Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PLZ}, t_{PHZ}	OC	ANY Q	50pF	2.0V			175		265		220	ns
			50pF	4.5V			35		53		44	
			50pF	6.0V			30		45		38	
t_r, t_f		ANY	50pF	2.0V			60		90		75	ns
			150pF	2.0V			210		315		265	
			50pF	4.5V			12		18		15	
			150pF	4.5V			42		63		53	
			50pF	6.0V			10		15		13	
			150pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per latch at 25°C	50 typ	pF

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called Q. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

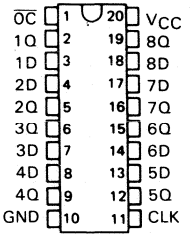
4

TYPES SN54HC374, SN74HC374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

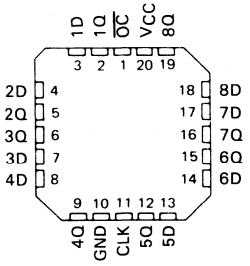
D2684, DECEMBER 1982

- **8 D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC374 . . . J PACKAGE
SN74HC374 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC374 . . . FH OR FK PACKAGE
SN74HC374 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

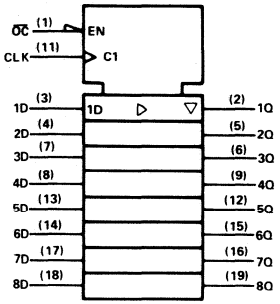
The eight flip-flops of the 'HC374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (OC) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC374 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC374			74HC374			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V	0		2	0		3	MHz
		4.5V	0		14	0		17	
		6.0V	0		16	0		20	
t_w	CLK high	2.0V	100			80			ns
		4.5V	20			16			
		6.0V	17			13			
	CLK low	2.0V	100			80			
		4.5V	20			16			
		6.0V	17			13			
t_{su}		2.0V	100			80			ns
		4.5V	20			16			
		6.0V	17			13			
t_h		2.0V	5			5			ns
		4.5V	5			5			
		6.0V	5			5			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

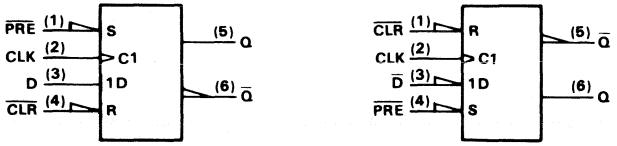
PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC374		74HC374		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max},			50pF	2.0V	4			2		3		MHz
			150pF	2.0V	4			2		3		
			50pF	4.5V	22			14		17		
			150pF	4.5V	22			14		17		
			50pF	6.0V	25			16		20		
			150pF	6.0V	25			16		20		
t_{PLH}, t_{PHL},	CLK	Q	50pF	2.0V			210		315		265	ns
			150pF	2.0V			295		445		370	
			50pF	4.5V			42		63		53	
			150pF	4.5V			59		89		74	
			50pF	6.0V			36		54		45	
			150pF	6.0V			51		76		64	
t_{PZH}, t_{PZL},	$\overline{OC}$	Q	50pF	2.0V			210		315		265	ns
			150pF	2.0V			295		445		370	
			50pF	4.5V			42		63		53	
			150pF	4.5V			59		89		74	
			50pF	6.0V			36		54		45	
			150pF	6.0V			51		76		64	
t_{PHZ}, t_{PLZ}	$\overline{OC}$	Q	50pF	2.0V			180		270		225	ns
			50pF	4.5V			36		54		45	
			50pF	6.0V			31		46		39	
t_r, t_f		ANY	50pF	2.0V			60		90		75	ns
			150pF	2.0V			210		315		265	
			50pF	4.5V			12		18		15	
			150pF	4.5V			42		63		53	
			50pF	6.0V			10		15		13	
			150pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per Flip-Flop at 25°C	85 typ	pF

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

4

TYPES SN54HC377, SN54HC378*, SN54HC379*, SN74HC377, SN74HC378*, SN74HC379* OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

D2684, DECEMBER 1982

- **'HC377 and 'HC378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs**
- **'HC379 Contains Four Flip-Flops with Double-Rail Outputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These circuits are positive-edge-triggered D-type flip-flops with an enable input. The 'HC377, 'HC378, and 'HC379 devices are similar to 'HC273, 'HC174, and 'HC175 respectively, but feature a common clock enable ($\overline{G}$) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

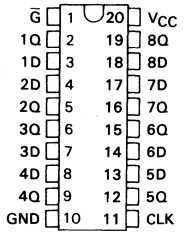
The SN54HC377, SN54HC378, and SN54HC379 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC377, SN74HC378, and SN74HC379 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

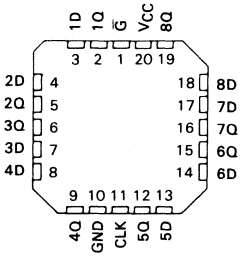
INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$†
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

†'HC379 only

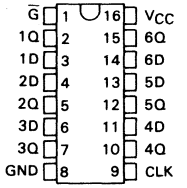
SN54HC377 . . . J PACKAGE
SN74HC377 . . . J OR N PACKAGE
(TOP VIEW)



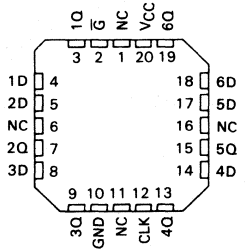
SN54HC377 . . . FH OR FK PACKAGE
SN74HC377 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC378 . . . J PACKAGE
SN74HC378 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC378 . . . FH OR FK PACKAGE
SN74HC378 . . . FH OR FN PACKAGE
(TOP VIEW)



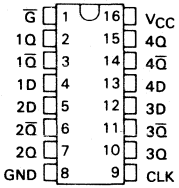
NC — No internal connection

*) **PRODUCT PREVIEW**

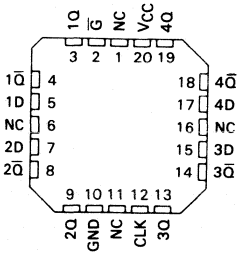
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

SN54HC379 . . . J PACKAGE
SN74HC379 . . . J OR N PACKAGE
(TOP VIEW)



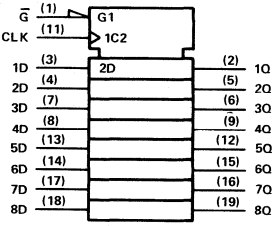
SN54HC379 . . . FH OR FK PACKAGE
SN74HC379 . . . FH OR FN PACKAGE
(TOP VIEW)



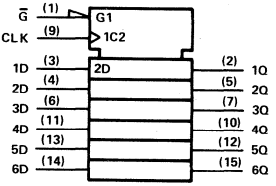
NC — No internal connection

logic symbols

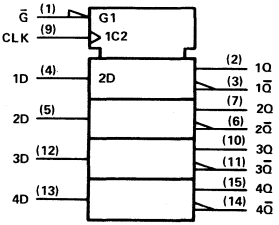
'HC377



'HC378



'HC379



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC377 MIN	54HC377 NOM	54HC377 MAX	74HC377 MIN	74HC377 NOM	74HC377 MAX	UNITS
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	CLK high or low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	D	2.0V 4.5V 6.0V	165 33 28			140 28 24			ns
	$\overline{G}$ low	2.0V 4.5V 6.0V	165 33 28			140 28 24			
	$\overline{G}$ high	2.0V 4.5V 6.0V	165 33 28			140 28 24			
t_h		2.0V 4.5V 6.0V	5 5 5			5 5 5			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC377		74HC377		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	CLK	ANY	2.0V 4.5V 6.0V			175 35 30		265 53 45		220 44 37	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance per flip-flop at 25°C	33 typ	pF

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC378			74HC378			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 16 19			4 20 23	MHz
t_w	CLK high or low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	D	2.0V 4.5V 6.0V	165 33 28			140 28 24			ns
	$\overline{G}$ low	2.0V 4.5V 6.0V	165 33 28			140 28 24			
	$\overline{G}$ high	2.0V 4.5V 6.0V	165 33 28			140 28 24			
t_h		2.0V 4.5V 6.0V	5 5 5			5 5 5			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC378		74HC378		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	CLK	ANY	2.0V 4.5V 6.0V			160 32 27		240 48 41		200 40 34	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		90 19 16	ns

C_{pd}	Power dissipation capacitance per flip-flop at 25°C	27 typ	pF

*) PRODUCT PREVIEW

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC379			74HC379			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}		2.0V 4.5V 6.0V			3 6 19			4 20 23	MHz
t_w	CLK high or low	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	D	2.0V 4.5V 6.0V	150 30 21			125 25 21			ns
	$\overline{G}$ low	2.0V 4.5V 6.0V	115 23 20			95 19 16			
	$\overline{G}$ high	2.0V 4.5V 6.0V	115 23 20			95 19 16			
t_h		2.0V 4.5V 6.0V	0 0 0			0 0 0			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC379		74HC379		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PLH}, t_{PHL}	CLK	ANY	2.0V 4.5V 6.0V	150 30 26			225 45 38		190 38 32		ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		90 19 16	ns

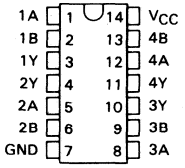
C_{pd}	Power dissipation capacitance per flip-flop at 25°C	30 typ	pF

TYPES SN54HC386, SN74HC386 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

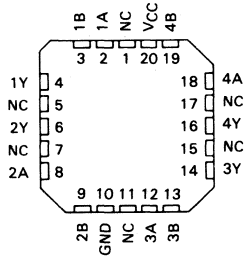
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC386 . . . J PACKAGE
SN74HC386 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC386 . . . FH OR FK PACKAGE
SN74HC386 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

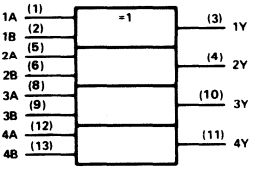
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC386 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC386 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC386		74HC386		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A or B	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r, t_f		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	40 typ	pF

TYPES SN54HC390, SN54HC393, SN74HC390, SN74HC393 DUAL 4-BIT DECADE AND BINARY COUNTERS

D2684, DECEMBER 1982

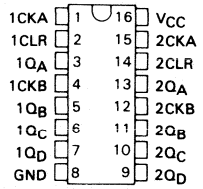
- **'HC390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters**
- **'HC393 . . . Dual 4-Bit Binary Counter with Individual Clocks**
- **All Have Direct Clear for Each 4-Bit Counter**
- **Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

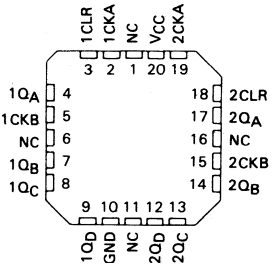
Each of these monolithic circuits contains eight flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'HC390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'HC393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'HC390 and 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

The SN54HC390 and SN54HC393 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC390 and SN74HC393 are characterized for operation from −40°C to 85°C.

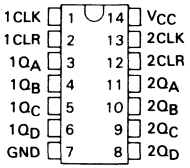
SN54HC390 . . . J PACKAGE
SN74HC390 . . . J OR N PACKAGE
(TOP VIEW)



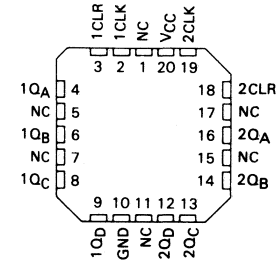
SN54HC390 . . . FH OR FK PACKAGE
SN74HC390 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC393 . . . J PACKAGE
SN74HC393 . . . J OR N PACKAGE
(TOP VIEW)



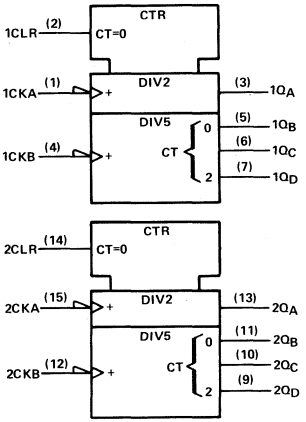
SN54HC393 . . . FH OR FK PACKAGE
SN74HC393 . . . FH OR FN PACKAGE
(TOP VIEW)



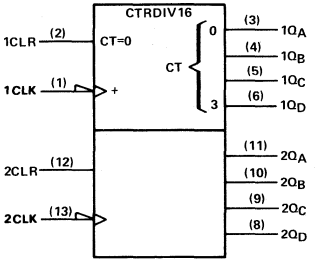
NC — No internal connection

logic symbols

'HC390



'HC393



Pin numbers shown are for J and N packages.

4

FUNCTION TABLES

'HC390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'HC390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'HC393
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.

timing requirements (supplement to recommended operating conditions)

PARAMETER		CONDITIONS V_{CC}	54HC390 54HC393			74HC390 74HC393			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	CKA or CLK	2.0V	0		3	0		4	MHz
		4.5V	0		16	0		20	
		6.0V	0		19	0		23	
	CKB	2.0V	150			125			
		4.5V	30			25			
		6.0V	25			21			
t_w	CKA or CLK HI or LO	2.0V	150			125			ns
		4.5V	30			25			
		6.0V	25			21			
	CKB high or low	2.0V	225			190			
		4.5V	45			38			
		6.0V	38			32			
	CLR high	2.0V	255			215			
		4.5V	51			43			
		6.0V	43			37			
t_{su}		2.0V	0			0			ns
		4.5V	0			0			
		6.0V	0			0			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC390 54HC393		74HC390 74HC393		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CKA or CLK	QA	2.0V	5			3		4		MHz
			4.5V	25			16		20		
			6.0V	29			19		23		
	CKB	QB	2.0V			215		325		270	
			4.5V			43		65		54	
			6.0V			37		55		46	
t_{PD}	CKA or CLK	QA	2.0V			205		310		255	ns
			4.5V			41		62		51	
			6.0V			35		53		43	
t_{PD}	CKA or CLK	QC	2.0V			195		295		245	ns
			4.5V			39		59		49	
			6.0V			33		50		42	
t_{PD}	CKB	QB	2.0V			210		315		265	ns
			4.5V			42		63		53	
			6.0V			36		54		45	
t_{PD}	CKB	QC	2.0V			220		330		275	ns
			4.5V			44		66		55	
			6.0V			37		56		47	
t_{PD}	CKB	QD	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_{PHL}	CLR	ANY	2.0V								ns
			4.5V								
			6.0V								

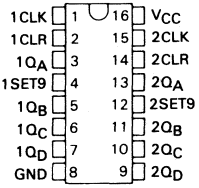
C_{pd}	Power dissipation capacitance per counter at 25°C	60 typ	pF

TYPES SN54HC490, SN74HC490
DUAL 4-BIT DECADE COUNTERS

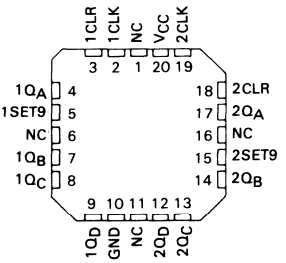
D2684, DECEMBER 1982

- **Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter**
- **Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC490 . . . J PACKAGE
SN74HC490 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC490 . . . FH OR FK PACKAGE
SN74HC490 . . . FH OR FN PACKAGE
(TOP VIEW)



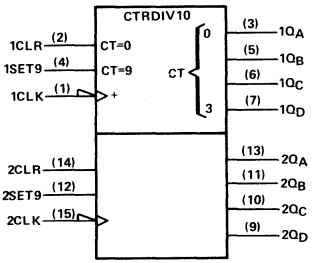
NC — No internal connection

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single 'HC490. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54HC490 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC490 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

CLEAR/SET-TO-9 FUNCTION TABLE (EACH COUNTER)

INPUTS		OUTPUTS			
CLEAR	SET-TO-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

BCD COUNT SEQUENCE (EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC490			74HC490			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	2.0V 4.5V 6.0V	0 0 0		3 16 19	0 0 0		4 20 23	MHz
t_w	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC490		74HC490		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2.0V 4.5V 6.0V	5 25 29			3 16 19		4 20 23		MHz
t_{PD}	CLK	QA	2.0V 4.5V 6.0V			215 43 37		325 65 55		270 54 46	ns
t_{PD}	CLK	QB, QD	2.0V 4.5V 6.0V			205 41 35		310 62 53		255 51 43	ns
t_{PD}	CLK	QC	2.0V 4.5V 6.0V			195 39 33		295 59 50		245 49 42	ns
t_{PLH}	SET-TO-9	QA, QD	2.0V 4.5V 6.0V			210 42 36		315 63 54		265 53 45	ns
t_{PHL}		QB, QC	2.0V 4.5V 6.0V			220 44 37		330 66 56		275 55 47	ns
t_r, t_f		ANY	2.0V 4.5V 6.0V			75 15 13		110 22 19		95 19 16	ns

C_{pd}	Power dissipation capacitance per counter at 25°C	60 typ	pF

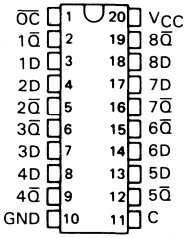
4

TYPES SN54HC533, SN74HC533
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

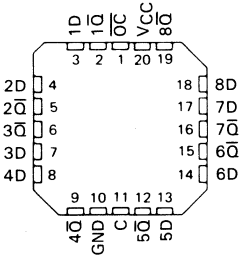
D2684, DECEMBER 1982

- **8 Latches In a Single Package**
- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC533 . . . J PACKAGE
SN74HC533 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC533 . . . FH OR FK PACKAGE
SN74HC533 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'HC533 is functionally equivalent to the 'HC373 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

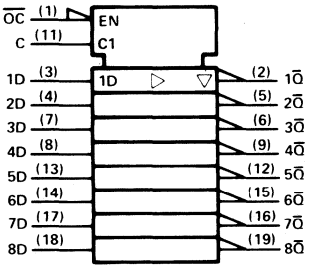
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC533 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC533 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC533			74HC533			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	2.0V	150			125			ns
	4.5V	30			25			
	6.0V	25			21			
t_{su}	2.0V							ns
	4.5V		TBD			TBD		
	6.0V							
t_h	2.0V							ns
	4.5V		TBD			TBD		
	6.0V							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

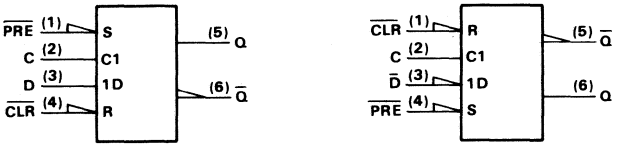
PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC533		74HC533		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	D	Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PLH}, t_{PHL}	C	ANY Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PZH}, t_{PZL}	OC	ANY Q	50pF	2.0V			175		265		220	ns
			150pF	2.0V			260		395		325	
			50pF	4.5V			35		53		44	
			150pF	4.5V			52		79		65	
			50pF	6.0V			30		45		38	
			150pF	6.0V			45		67		57	
t_{PLZ}, t_{PHZ}	OC	ANY Q	50pF	2.0V			175		265		220	ns
			50pF	4.5V			35		35		44	
			50pF	6.0V			30		30		38	
t_r, t_f		ANY	50pF	2.0V			60		90		75	ns
			150pF	2.0V			210		315		265	
			50pF	4.5V			12		18		15	
			150pF	4.5V			42		63		53	
			50pF	6.0V			10		15		13	
			150pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per latch at 25°C	typ	pF

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

4

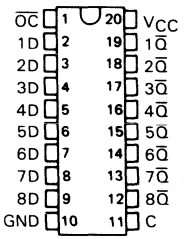
HIGH-SPEED CMOS LOGIC

TYPES SN54HC563, SN74HC563 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

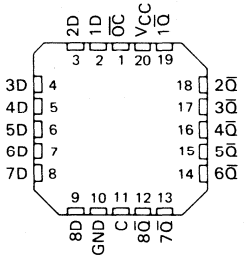
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC563 . . . J PACKAGE
SN74HC563 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC563 . . . FH OR FK PACKAGE
SN74HC563 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the outputs will be latched at the inverses of the levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

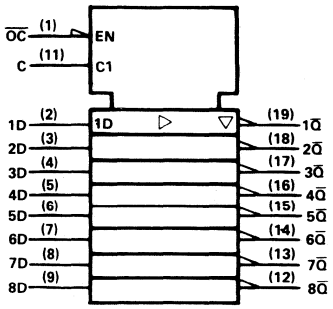
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC563 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(Each Latch)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC563 54HCT563			74HC563 74HCT563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	2.0V 4.5V 6.0V		TBD			TBD		ns
t_h	2.0V 4.5V 6.0V		TBD			TBD		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

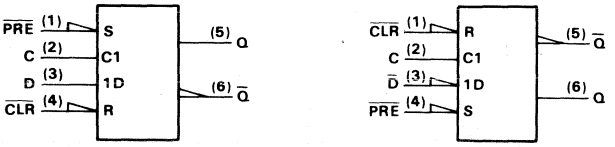
PARAMETER	FROM	TO	Conditions		$T_A = 25°C$			54HC563 54HCT563		74HC563 74HCT563		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	D	Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PLH}, t_{PHL}	C	ANY Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PZH}, t_{PZL}	$\overline{OC}$	ANY Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PLZ}, t_{PHZ}	$\overline{OC}$	ANY Q	50 pF 50 pF 50 pF	2.0V 4.5V 6.0V			175 35 30		265 35 30		220 44 38	ns
t_r, t_f		ANY	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			60 210 12 42 10 36		90 315 18 63 15 53		75 265 15 53 13 45	ns

C_{pd}	Power dissipation capacitance per latch at 25°C	typ	pF

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊐) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

4

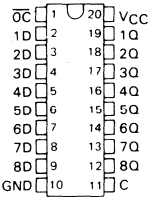
TYPES SN54HCT573, SN74HCT573, SN54HC573, SN74HC573
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

HIGH-SPEED CMOS LOGIC

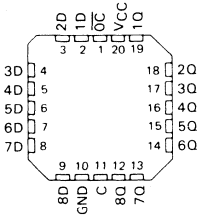
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC573 . . . J PACKAGE
SN74HC573 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC573 . . . FH OR FK PACKAGE
SN74HC573 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

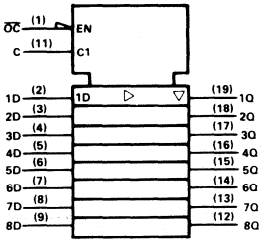
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54HC573 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC573 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

timing requirements (supplement to recommended operating conditions)

PARAMETER	CONDITIONS V_{CC}	54HC573 54HCT573			74HC573 74HCT573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	2.0V 4.5V 6.0V	150 30 25			125 25 21			ns
t_{su}	2.0V 4.5V 6.0V		TBD			TBD		ns
t_h	2.0V 4.5V 6.0V		TBD			TBD		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

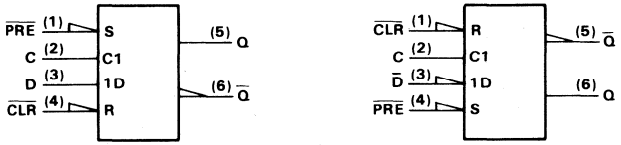
PARAMETER	FROM	TO	Conditions		$T_A = 25°C$			54HC573 54HCT573		74HC573 74HCT573		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PD}	D	Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PD}	C	ANY Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PZH}, t_{PZL}	$\overline{OC}$	ANY Q	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			175 260 35 52 30 45		265 395 53 79 45 67		220 325 44 65 38 57	ns
t_{PLZ}, t_{PHZ}	$\overline{OC}$	ANY Q	50 pF 50 pF 50 pF	2.0V 4.5V 6.0V			175 35 30		265 35 30		220 44 38	ns
t_t		ANY	50 pF 150 pF 50 pF 150 pF 50 pF 150 pF	2.0V 2.0V 4.5V 4.5V 6.0V 6.0V			60 210 12 42 10 36		90 315 18 63 15 53		75 265 15 53 13 45	ns

C_{pd}	Power dissipation capacitance per latch at 25°C	typ	pF

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

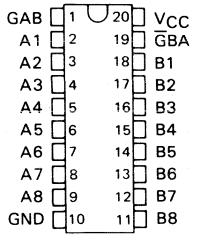
TYPES SN54HC620*, SN54HC623, SN74HC620*, SN74HC623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

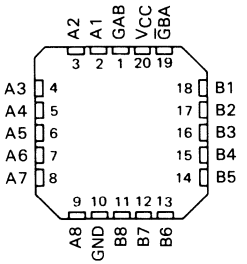
- **Bus Transceivers in High-Density 20-Pin DIPs and also Plastic and Ceramic Chip Carriers**
- **Lock Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC620	Inverting
'HC623	True

SN54HC' . . . J PACKAGE
SN74HC' . . . J OR N PACKAGE
(TOP VIEW)



SN54HC' . . . FH OR FK PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HC623 or complementary for the 'HC620.

The SN54HC620 and SN54HC623 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC620 and SN74HC623 are characterized for operation from -40°C to 85°C.

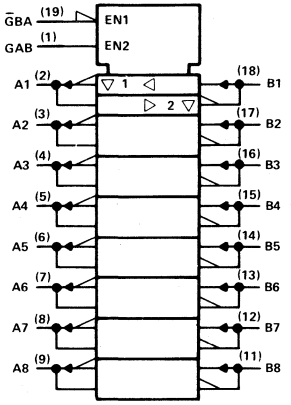
FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'HC620	'HC623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

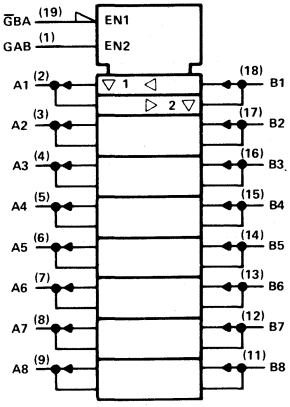
*) **PRODUCT PREVIEW**

logic symbols

'HC620



'HC623



Pin numbers shown are for J and N packages.

4

'HC620 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC620		74HC620		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PZH}	$\overline{G}$BA	A	50 pF	2.0V			210		315		265	ns
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PZL}			50 pF	2.0V			210		315		265	
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PLZ}	$\overline{G}$BA	A	50 pF	2.0V			125		190		155	ns
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PHZ}			50 pF	2.0V			125		190		155	
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PZH}	GAB	B	50 pF	2.0V			210		315		265	ns
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PZL}			50 pF	2.0V			210		315		265	
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PLZ}	GAB	B	50 pF	2.0V			125		190		155	ns
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PHZ}			50 pF	2.0V			125		190		155	
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per TXCVR at 25°C	typ	pF

4

'HC623 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC623		74HC623		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PZH}	$\overline{G}BA$	A	50 pF	2.0V			210		315		265	ns
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PZL}			50 pF	2.0V			210		315		265	
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			91		76		64	
t_{PLZ}	$\overline{G}BA$	A	50 pF	2.0V			125		190		155	ns
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PHZ}			50 pF	2.0V			125		190		155	
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PZH}	GAB	B	50 pF	2.0V			210		315		265	ns
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PZL}			50 pF	2.0V			210		315		265	
			150 pF	2.0V			295		445		370	
			50 pF	4.5V			42		63		53	
			150 pF	4.5V			59		89		74	
			50 pF	6.0V			36		54		45	
			150 pF	6.0V			51		76		64	
t_{PLZ}	GAB	B	50 pF	2.0V			125		190		155	ns
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_{PHZ}			50 pF	2.0V			125		190		155	
			50 pF	4.5V			25		38		31	
			50 pF	6.0V			21		32		26	
t_r	A or B		50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per TXCVR at 25°C	typ	pF

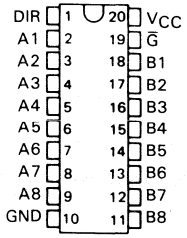
TYPES SN54HC640*, SN54HC643
SN74HC640*, SN74HC643
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

- **Bus Transceivers in High-Density 20-Pin DIPs and also Plastic and Ceramic Chip Carriers**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC640	Inverting
'HC643	True and Inverting

SN54HC' . . . J PACKAGE
SN74HC' . . . J OR N PACKAGE
(TOP VIEW)

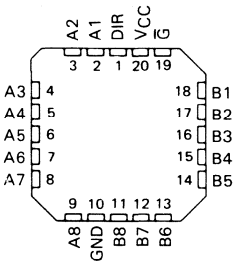


description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The SN54HC640 and SN54HC643 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC640 and SN74HC643 are characterized for operation from −40°C to 85°C.

SN54HC' . . . FH OR FK PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



4

FUNCTION TABLE

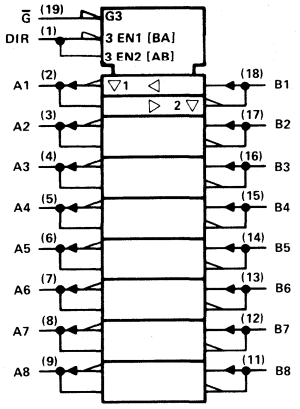
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'HC640	'HC645	'HC643
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

*) PRODUCT PREVIEW

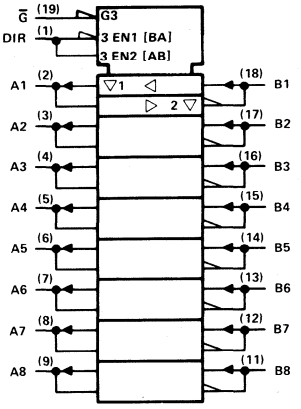
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbols

'HC640



'HC643



Pin numbers shown are for J and N packages

4

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		$T_A = 25°C$			54HC640		74HC640		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	50 pF	2.0V			105		160		130	ns
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PHL}			50 pF	2.0V			105		160		130	
			150 pF	2.0V			190		290		235	
			50 pF	4.5V			21		32		26	
			150 pF	4.5V			38		58		47	
			50 pF	6.0V			18		27		22	
			150 pF	6.0V			33		49		41	
t_{PZH}	$\overline{G}$	A or B	50 pF	2.0V			230		340		290	ns
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PZL}			50 pF	2.0V			230		340		290	
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PLZ}	$\overline{G}$	A or B	50 pF	2.0V			135		205		170	ns
			50 pF	4.5V			27		41		34	
			50 pF	6.0V			23		35		29	
t_{PHZ}			50 pF	2.0V			135		205		170	
			50 pF	4.5V			27		41		34	
			50 pF	6.0V			23		35		29	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

C_{pd}	Power dissipation capacitance per TXCVR at 25°C	typ	pF

4

'HC643 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS		T_A = 25°C			54HC643		74HC643		UNIT
			C_L	V_{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	B	50 pF	2.0V			110		165		140	ns
			150 pF	2.0V			195		295		245	
			50 pF	4.5V			22		33		28	
			150 pF	4.5V			39		59		49	
			50 pF	6.0V			19		28		24	
			150 pF	6.0V			34		50		43	
t_{PLH}, t_{PHL}	B	A	50 pF	2.0V			110		165		140	ns
			150 pF	2.0V			195		295		245	
			50 pF	4.5V			22		33		28	
			150 pF	4.5V			39		59		49	
			50 pF	6.0V			19		28		24	
			150 pF	6.0V			34		50		43	
t_{PZH}, t_{PZL}	$\overline{G}$	A	50 pF	2.0V			230		340		290	ns
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PZH}, t_{PZL}	$\overline{G}$	B	50 pF	2.0V			230		340		290	ns
			150 pF	2.0V			315		470		395	
			50 pF	4.5V			46		68		58	
			150 pF	4.5V			63		94		79	
			50 pF	6.0V			39		58		49	
			150 pF	6.0V			54		80		68	
t_{PLZ}, t_{PHZ}	$\overline{G}$	A	50 pF	2.0V			135		205		170	ns
			50 pF	4.5V			27		41		34	
			50 pF	6.0V			23		35		29	
t_{PHZ}, t_{PLZ}	$\overline{G}$	B	50 pF	2.0V			135		205		170	ns
			50 pF	4.5V			27		41		34	
			50 pF	6.0V			23		35		29	
t_r		A or B	50 pF	2.0V			60		90		75	ns
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	
t_f			50 pF	2.0V			60		90		75	
			150 pF	2.0V			210		315		265	
			50 pF	4.5V			12		18		15	
			150 pF	4.5V			42		63		53	
			50 pF	6.0V			10		15		13	
			150 pF	6.0V			36		53		45	

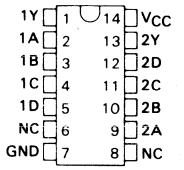
C_{pd}	Power dissipation capacitance per TXCVR at 25°C	typ	pF

TYPES SN54HC4002, SN74HC4002
DUAL 4-INPUT POSITIVE-NOR GATES

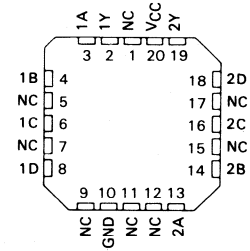
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4002 . . . J PACKAGE
SN74HC4002 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4002 . . . FH OR FK PACKAGE
SN74HC4002 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

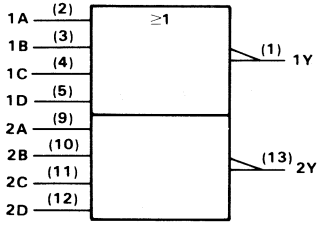
These devices contain two independent 4-input positive-NOR gates. They perform the boolean functions $Y = \overline{A + B + C + D}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ in positive logic.

The SN54HC4002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4002 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF, T_A = 25°C			54HC4002		74HC4002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A thru D	Y	2.0V			110		165		140	ns
			4.5V			22		33		28	
			6.0V			19		28		24	
t_{PHL}			2.0V			110		165		140	
			4.5V			22		33		28	
			6.0V			19		28		24	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

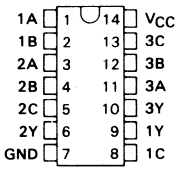
C_{pd}	Power dissipation capacitance per gate at 25°C	25 typ	pF

TYPES SN54HC4075, SN74HC4075
TRIPLE 3-INPUT OR GATES

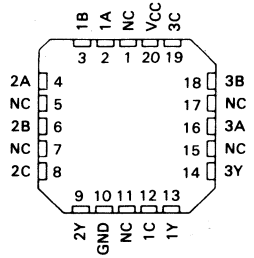
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4075 . . . J PACKAGE
SN74HC4075 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4075 . . . FH OR FK PACKAGE
SN74HC4075 . . . FH OR FN PACKAGE
(TOP VIEW)



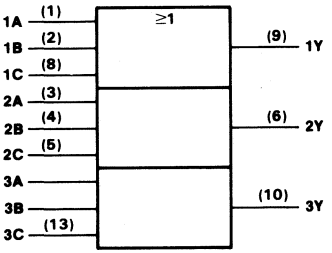
NC — No internal connection

description

These devices contain three independent 3-input OR gates and perform the boolean functions $Y = A + B + C$ or $Y = \overline{A \cdot B \cdot C}$ in positive logic.

The SN54HC4075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4075 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC4075		74HC4075		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or, C	Y	2.0V			100		150		125	ns
			4.5V			20		30		25	
			6.0V			17		25		21	
t_{PHL}			2.0V			100		150		125	
			4.5V			20		30		25	
			6.0V			17		25		21	
t_r		Y	2.0V			75		110		95	ns
			4.5V			15		22		19	
			6.0V			13		19		16	
t_f			2.0V			75		110		95	
			4.5V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	26 typ	pF

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

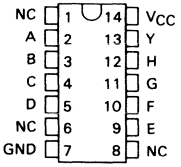
TEXAS INSTRUMENTS

TYPES SN54HC4078, SN74HC4078
8-INPUT NOR GATE

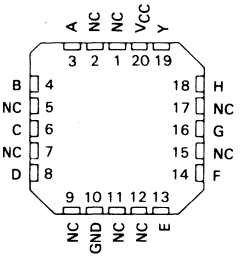
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4078 . . . J PACKAGE
SN74HC4078 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4078 . . . FH OR FK PACKAGE
SN74HC4078 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain a single 8-input NOR gate and perform the following boolean functions in positive logic:

$$Y = \overline{A + B + C + D + E + F + G + H} \text{ or}$$

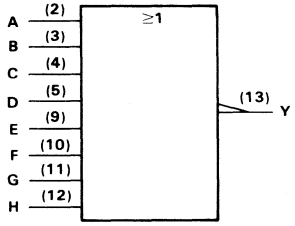
$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{H}$$

The SN54HC4078 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4078 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs L	H
One or more inputs H	L

logic symbol



Pin numbers shown are for J and N packages.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	CONDITIONS V_{CC}	C_L = 50 pF							UNIT
				T_A = 25°C			54HC4078		74HC4078		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A thru H	Y	2.0V			130		165		195	ns
			4.5V			26		33		39	
			6.0V			22		28		33	
t_r, t_f		Y	2.0V			75		110		95	ns
			2.0V			15		22		19	
			6.0V			13		19		16	

C_{pd}	Power dissipation capacitance per gate at 25°C	26 typ	pF

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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Explanation of Logic Symbols

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If you have questions on this Explanation of Logic Symbols, please contact:

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Dallas, Texas 75265
Telephone (214) 995-2867

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers,
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

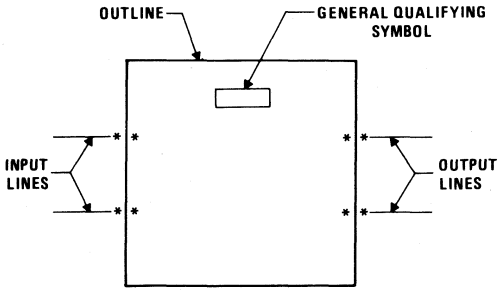
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

5

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

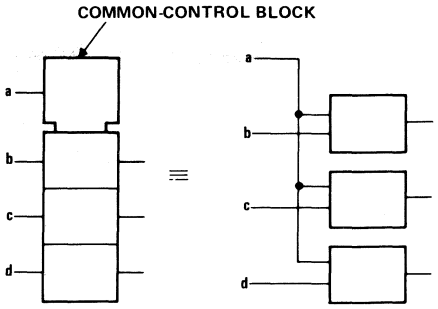


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

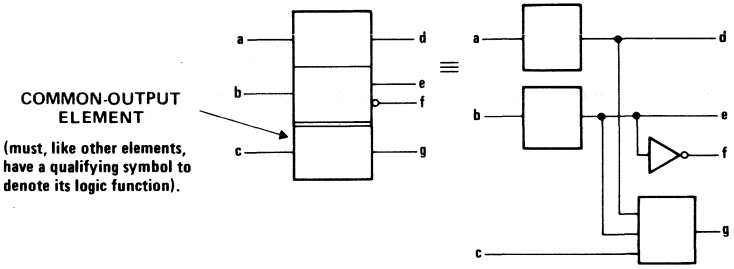


FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

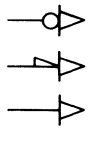
EXPLANATION OF LOGIC SYMBOLS

TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	'HC00
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86
=	Logic identity. All inputs must stand at same state.	'HC86
2k	An even number of inputs must be active.	'HC280
2k+1	An odd number of inputs must be active.	'HC86
1	The one input must be active.	'HC04
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240
⊓	Schmitt trigger; element with hysteresis.	'HC132
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	'HC42
MUX	Multiplexer/data selector.	'HC151
DMUX or DX	Demultiplexer.	'HC138
Σ	Adder.	*
P–Q	Subtracter.	*
CPG	Look-ahead carry generator.	*
π	Multiplier.	*
COMP	Magnitude comparator.	'HC85
ALU	Arithmetic logic unit.	*
⎍	Retriggerable monostable.	'HC123
1⎍	Non-retriggerable monostable (one-shot).	'HC221
G	Astable element. Showing waveform is optional.	*
!G	Synchronously starting astable.	*
G!	Astable element that stops with a completed pulse.	*
SRGm	Shift register. m = number of bits.	'HC164
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590
CTR DIVm	Counter with cycle length = m.	'HC160
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020
ROM	Read-only memory.	*
RAM	Random-access read/write memory.	'HC189
FIFO	First-in, first-out memory.	*
I=0	Element powers up cleared to 0 state.	*
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

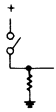
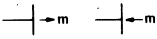
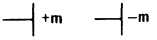
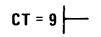
TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to  in positive logic.
	Active-low output. Equivalent to  in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition. POSITIVE LOGIC: 1→0 not used 0→1. NEGATIVE LOGIC: 0→1 not used 1→0. POLARITY INDICATION: not used H→L L→H
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
	Bi-threshold input (input with hysteresis)
	Open-drain or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to open-drain output but is suplemented with a built-in passive pull-up.
	Open-source or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to open-source output but is supplemented with a built-in passive pull-down.
	3-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-drain and open-source outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

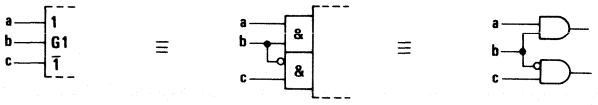


FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

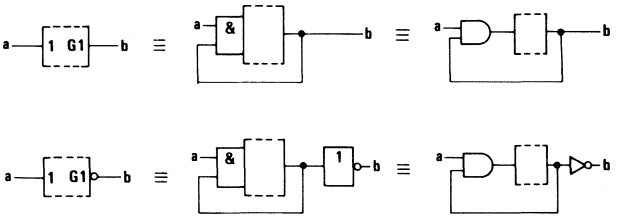


FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

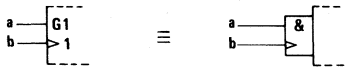


FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen; and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

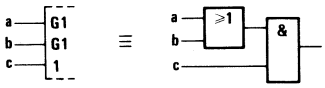


FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

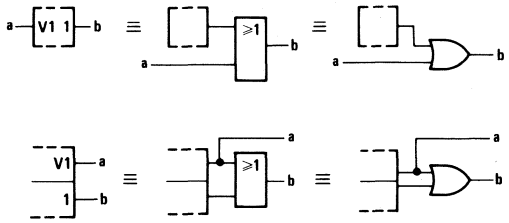


FIGURE 9 – V (OR) DEPENDENCY

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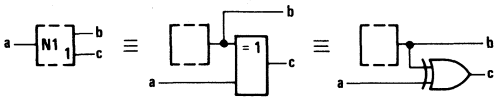
When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = b

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

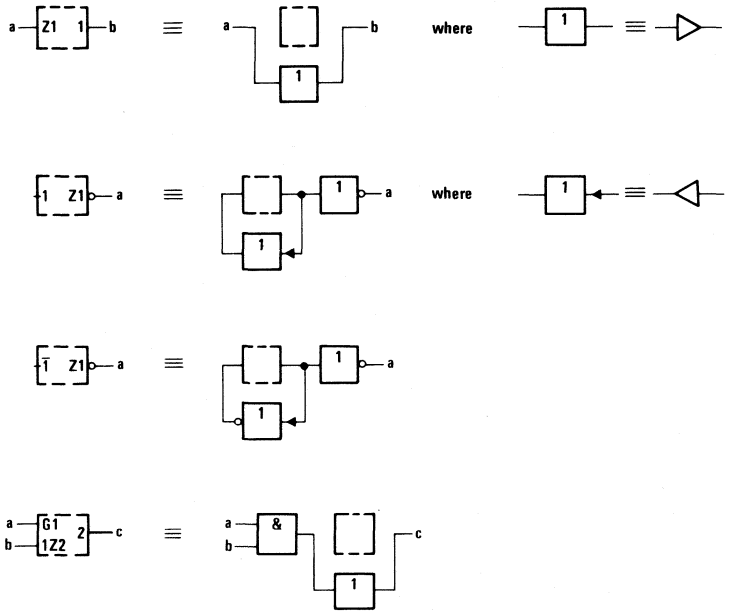
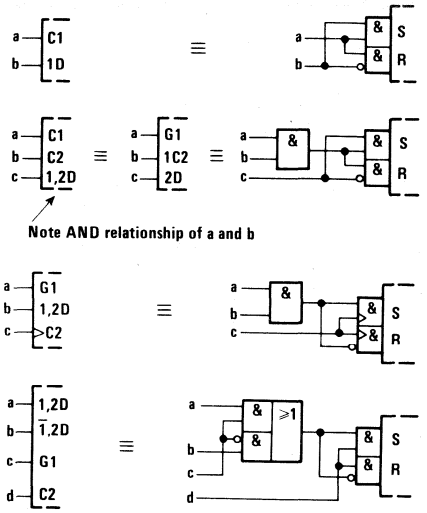


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.



Input c selects which of a or b is stored when d goes low.

FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

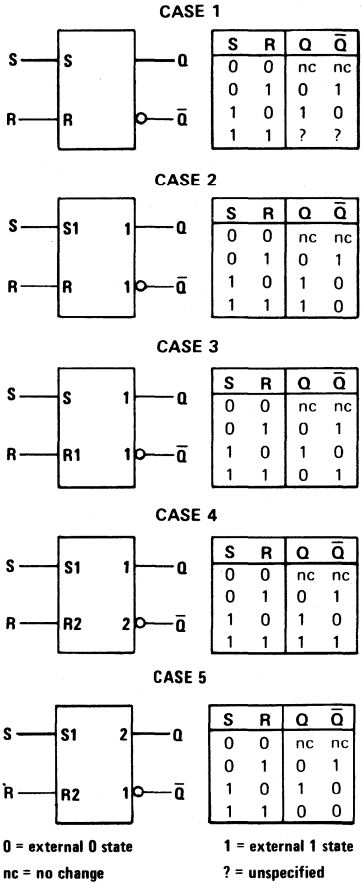
Set and reset dependencies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

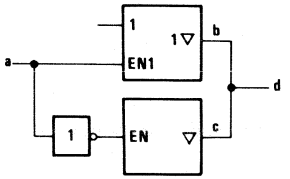
FIGURE 13 – S (SET) AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

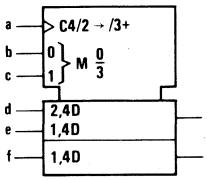
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

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4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

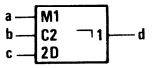


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

In Figure 17, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

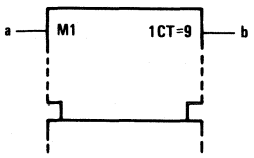


FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

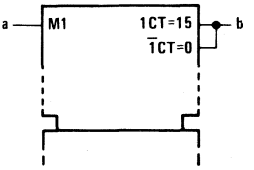


FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

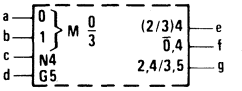


FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

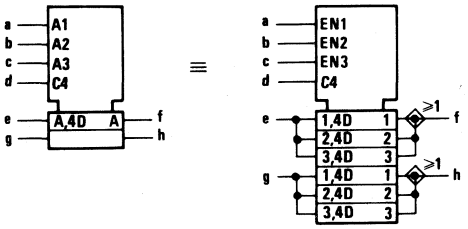


FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

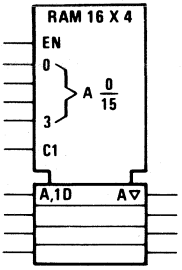


FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

5

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

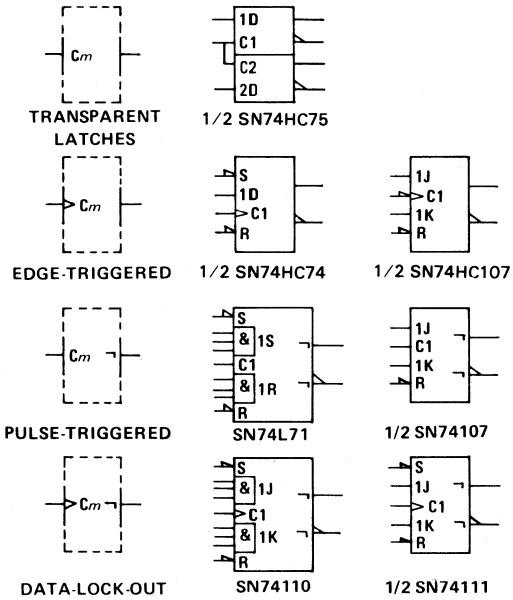


FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

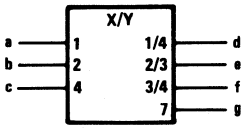
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

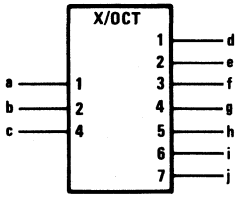
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



FUNCTION TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



FUNCTION TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

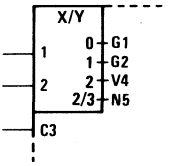


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

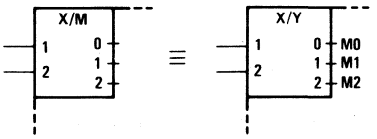


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

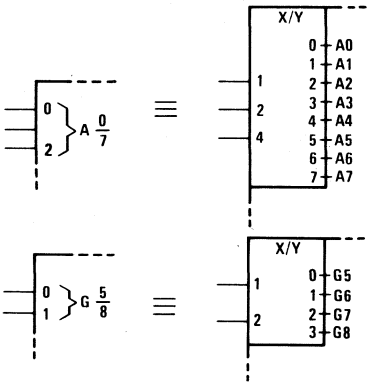


FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

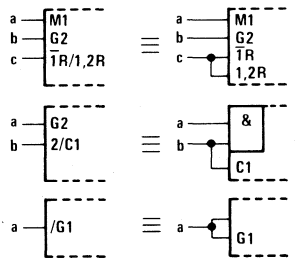


FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

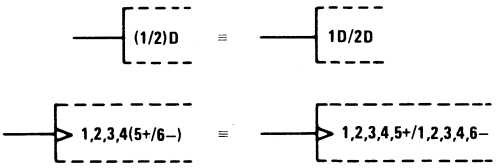


FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

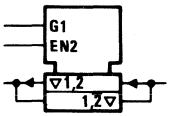


FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

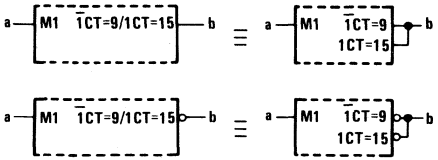


FIGURE 32 – OUTPUT LABELS

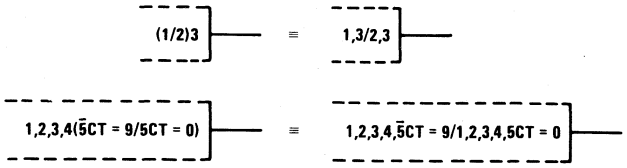


FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of Logic Symbols, please contact:

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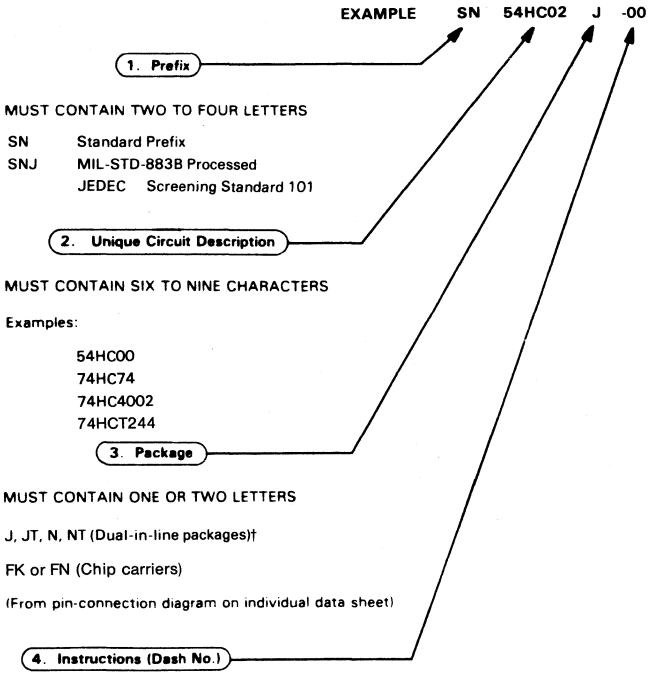
Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



† These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs

Dual-in-line (J, JT, N, NT)

- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier (N only)
- Sectioned Cardboard Box
- Individual Plastic Box

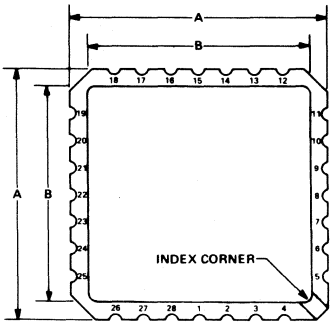
6

FK ceramic chip carrier packages

The FK package has a three-layer base with a metal lid and braze seal, and a ceramic base.

The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

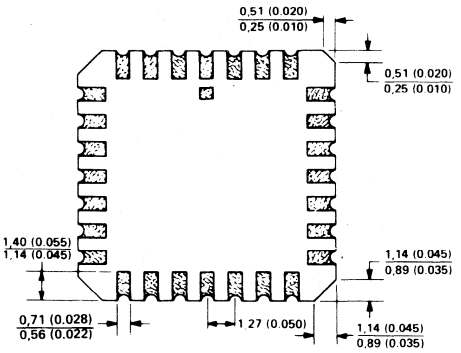
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)

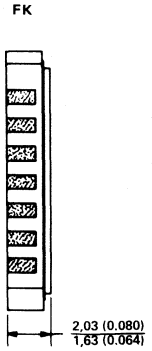


CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,93 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply.





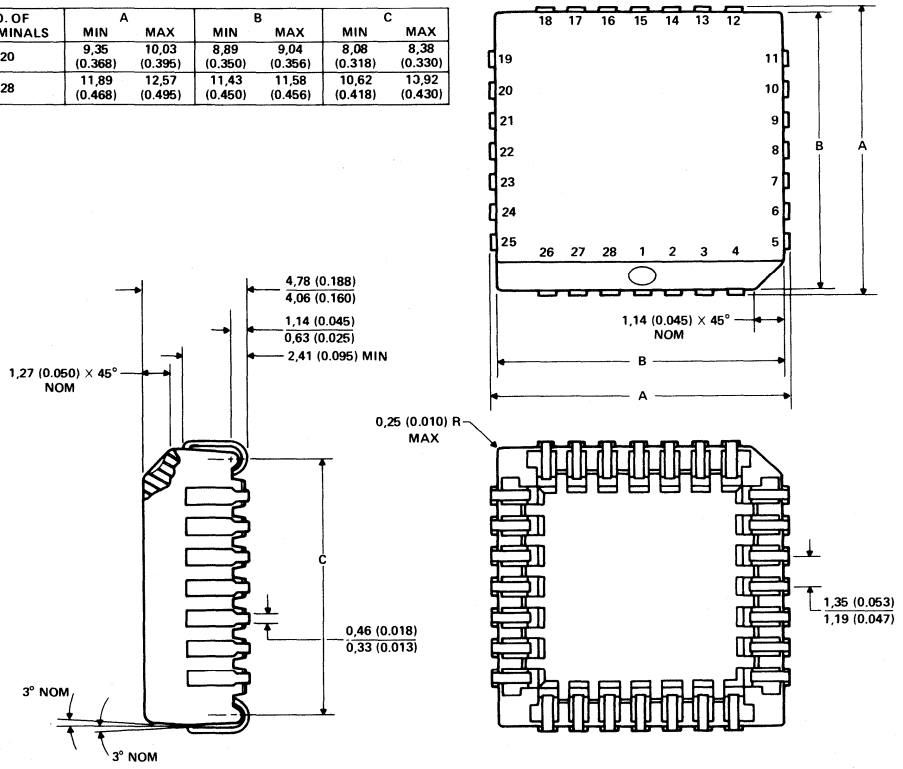
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,35 (0.368)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	11,89 (0.468)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)



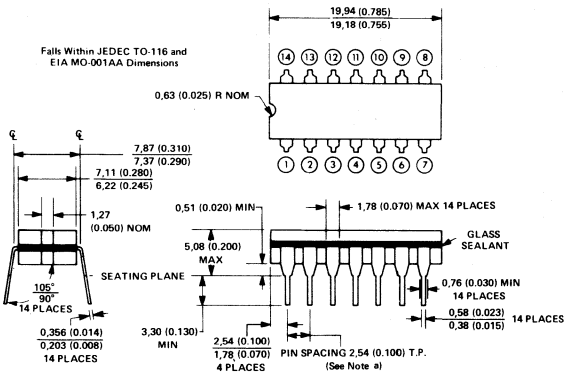
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

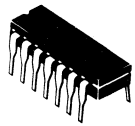
J ceramic packages (including JT packages)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing.

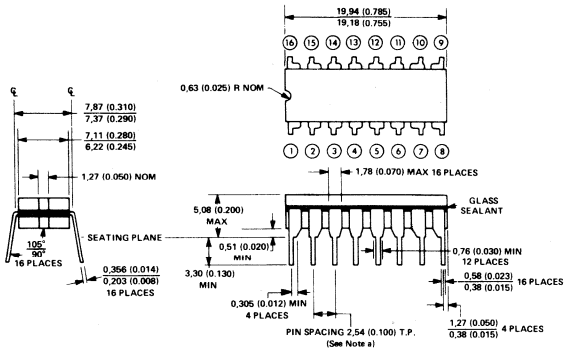
14-PIN J CERAMIC

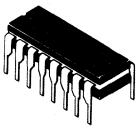




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

16-PIN J CERAMIC



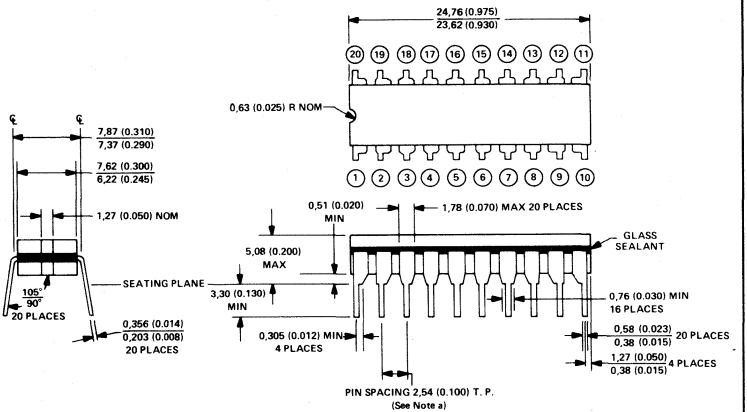


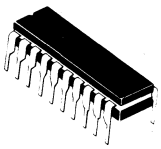
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

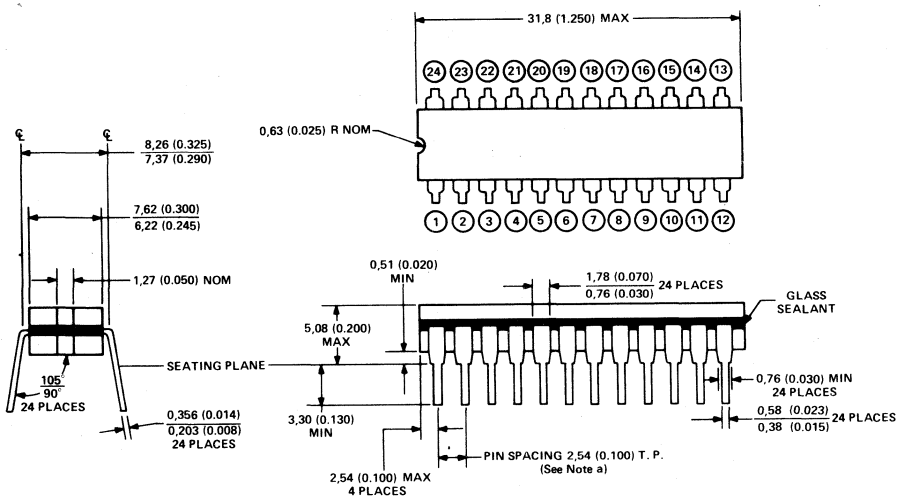
20-PIN J CERAMIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN JT CERAMIC



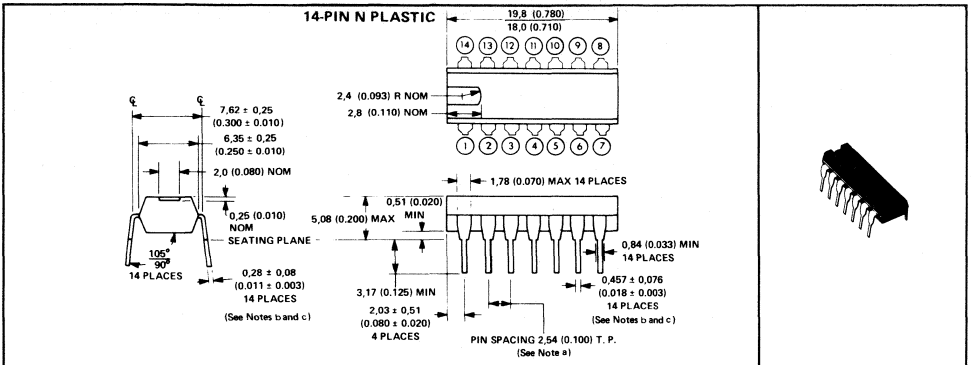
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

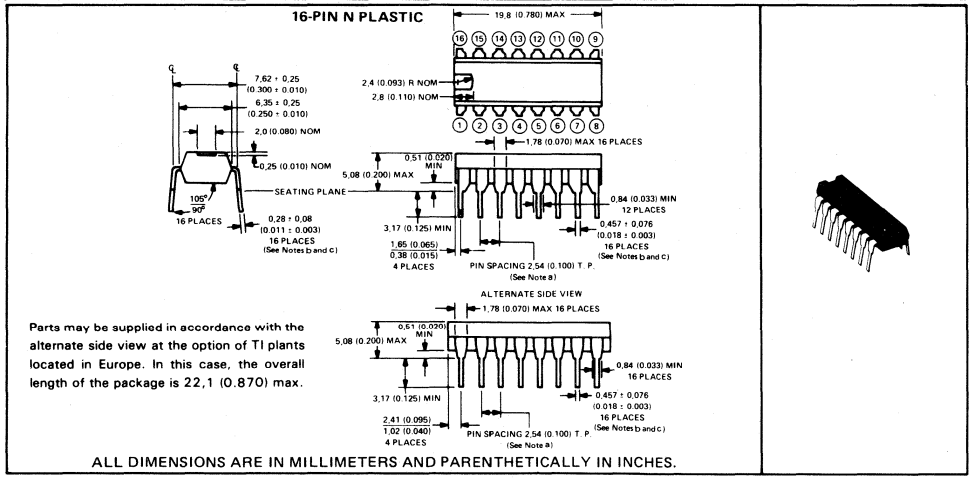
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic packages (including NT package)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically conductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width — 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package.

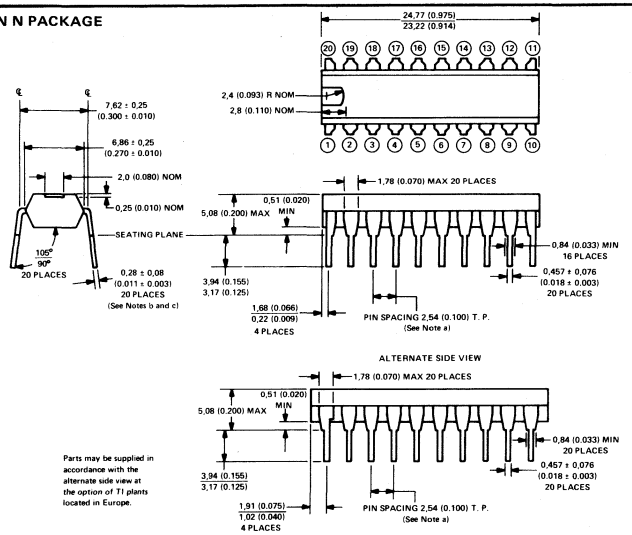




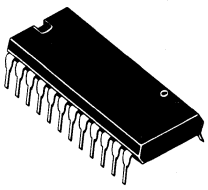
NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

20-PIN N PACKAGE

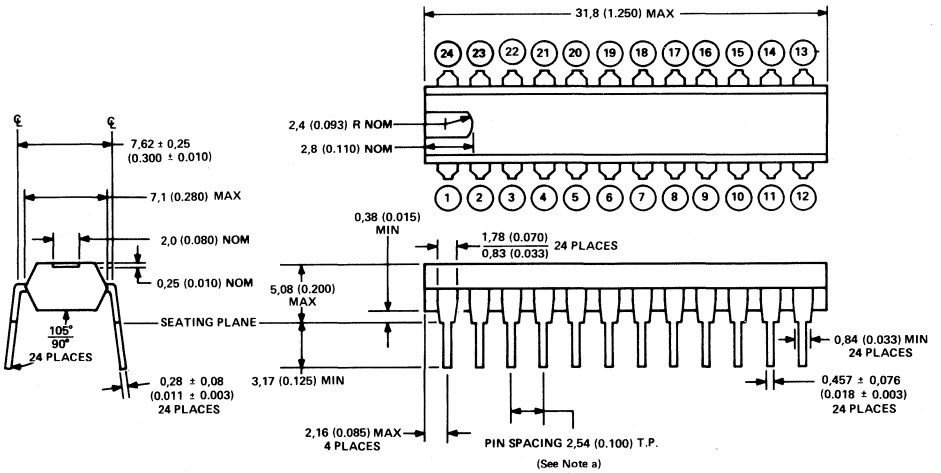


Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe.



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

24-PIN NT PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

b. This dimension does not apply for solder-dipped leads.

c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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